ARMY RESEARCH LABORATORY

# Chip on Glass Technology for Flat Panel Displays

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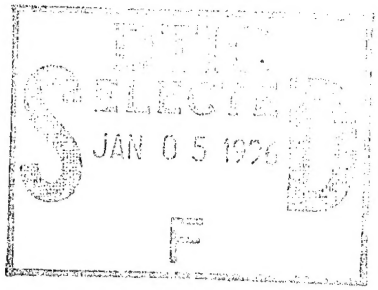
ARL-CR-258 November 1995




prepared by
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The goal of this contract was to apply chip on glass wire bonding and connection techniques to flat panel displays. This would considerably lower the cost of completed panels by eliminating individual driver chip packaging and as many as 3000 connections for a 640 x 480 pixel display. In addition, there would be benefits in size and reliability. The effort was able to successfully demonstrate that the process could be compatible with the structure and materials present in a flat panel display. A number of displays were fabricated and tested. The reliability of the drive chips proved to be a limiting factor, due to insufficient testing before installation. At present it is cost effective for displays smaller than 640 x 480; however, as the quality of the chips increases, it is expected to become cost effective to use the techniques developed in this program for larger displays.

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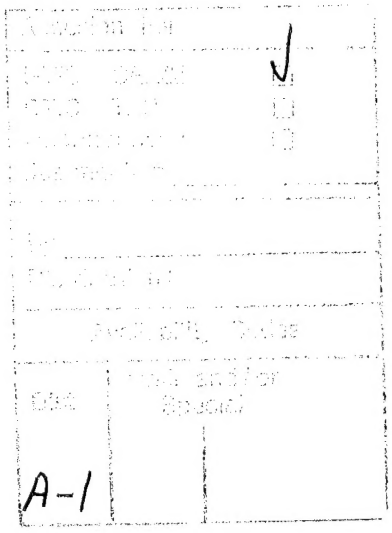


# 1. Introduction

## 1.1. Executive Summary

The SBIR Phase-II Development of Chip On Glass (COG) technology for Flat Panel Displays started in April of 1993 and continued through December 1994. The objectives were to install a pilot COG assembly line, and to design and build a TFEL VGA display to demonstrate the benefits of COG technology. The results of the Phase-I activities showed that the higher density and lower cost COG interconnect technology for smaller displays was highly desirable.

During the Phase-II contract the equipment for COG assembly was purchase and installed. The equipment was modified to handle the large VGA displays. The process was then debugged and optimized for the thin film metallurgy that is used on TFEL displays. Two displays were designed to use COG technology. The first was an EL640.480 gray scale VGA display that had 32 driver IC's attached with COG. The second display was an EL320.256 full color 1/4 VGA display that had 31 driver IC's. Over 60 of the EL320.256 displays were built, and the over 20 of the EL640.480 displays were built.

Three EL640.480 displays were delivered to the ARL as part of this contract. The displays were designed to be driven in a gray scale mode. The large display area put severe power requirements on the driver IC's. The high power requirements, as well as the yield and reliability of the gray scale drivers necessitated driving the displays in an on-off mode. The final displays delivered to ARL were driven in on-off mode.

**Conclusions**

The Chip-on-Glass (COG) interconnect technology was difficult to implement on large TFEL displays because of low driver IC yield, and the low conductivity of the bus. The first pass yield for the pilot production run of the color display using COG was 35%, due to driver failures. The COG technology is not well suited to the large area or high chip count EL displays.

The actual wire bonding of driver IC's to glass was successful and the process windows for COG on EL glass metals were very wide. Therefore, the target application for the COG technology at Planar is smaller displays with fewer driver IC's.

## 1.2. Acknowledgments

There are many people that worked on this technology development and implementation effort. Dr. Chris King, Scott Cockey, and Candice Brown submitted the original proposal. Preston Lewis, Steve Coon, John Duncan, and

Larry Kunkler contributed to the equipment installation, equipment modifications, and equipment debug. Bob Zimmerman created some inventive methods for material handling, and Pat Green helped to document the process flow. Davar Roshanagh designed the glass and tools for the monochrome VGA display, and also developed the encapsulation process. Karen Boris operated the equipment during the pilot production run. Tim Flegal and Allan Douglas designed the electronics and Tim Flegal wrote the electrical design section (section 6) of this report.

The ARL was instrumental in making the COG development effort possible. The ARL funded this SBIR-II project starting in July 1993 for a total of $500,000 . Richard Tuttle, David Chiu, and Robert Miller gave technical insight and direction for the project, and Lisa Williams was our administrative contact at the ARL.

## 2. Technology

### 2.1. Interconnects

Several different interconnect technologies are currently being used at Planar to connect the drive electronics to the EL glass. There are also several new technologies that we are investigating that will address the future requirements of EL displays. The technologies are listed here and a brief description for each is given in the text that follows.

Interconnect Technologies

- Elastomeric Connectors
- Lead Frame
- Heat Seal Connectors (HSC)
- TAB Film-on-Glass (FOG)
- Wire Bonded Chip-on-Glass (COG)
- Flip-Chip-on-Glass (FCOG)

Elastomeric Connectors: This is one of the most used interconnect technologies at Planar. It consists of a foam strip with annular rings of conductors. The strip is compressed between the glass and the circuit board pads, forming the electrical connection in the Z direction only. One major benefit of these connections are that they are very easy to rework with no loss of good components in the system. The other benefit of this technology is that the interconnects can be scaled independent of the driver IC's that is on the circuit board. Also, these are room temperature mechanical connections. The major disadvantage of the Elastomeric technology is the cost and the limited I/O density that can be achieved.

Lead Frame: The lead frame technology consists of a clip of metal leads that are soldered both to the glass metals and to the circuit board. The benefit of this technology is that the solder joints are proven reliable, and this technology can also be scaled to various display sizes. The challenges are that the lead frame technology is I/O limited, requires high temperatures, and is fairly labor intensive.

Heat Seal Connectors: The heat seal connectors (HSC) are a family of interconnect that have the characteristics of an anisotropic conductive film (ACF) built into the connecting ends of a flex cable structure. The interconnect is made with a relatively low temperature and pressure. The only critical part of the process is the alignment of the flex cable to the glass and circuit board. The benefits of this technology is that the connection is flexible, that is, it can be bent and formed into various configurations. The HSC technology also allows for a small shelf area on the glass. And the last significant benefit, like the previous interconnect technologies mentioned, the HSC can be scaled. Some of the challenges when using the HSC technology are susceptibility to long term exposure to moisture. The HSC technology is also I/O limited.

FOG, TCP or TAB: The Tape Carrier Package (TCP) or in other words, IC drivers that are packaged using Tape Automated Bonding (TAB) are well suited for the display industry. Sometimes the terms FOG (Film on Glass) is used to describe the use of TCP on displays. The TCP consist of IC drivers that are gold bumped and thermocompression bonded to gold plated copper supported by polyimide. The input side is usually soldered to a bus card and the input side is attached to the glass metallurgy using Anisotropic Conductive Film (ACF). The advantage of using TCP technology is that the TCP has a very low profile. These TCP are typically higher I/O than the plastic packaged driver IC's that are found on the circuit boards. The TCP can go to very fine pitch. The TCP assembly process can be automated for glass assembly. These IC can be fully tested in the TCP package. Some of the many challenges with the TCP technology are that there are many capital intensive assembly operations. Added hardware is typically required. The package can not be scaled, and each new design has a significant NRE (non recurring expense) associated with it. This technology is well suited for few part numbers and high volumes.

COG: Chip on Glass (COG) consists of a driver IC in bare die form that is attached to glass with bond pads up, and then wire bonded to the glass. The metallurgy on the glass supply the input power and signals, as well as the output signals. The advantage of the COG technology is that this is the industry standard method for going from the IC's to the next level of packaging. Also IC's are readily available in this standard form, and pad metallurgy. And one last benefit is that this technology can be a low cost approach by eliminating the plastic or TCP package. The one overriding disadvantages of this technology is the difficulty of getting tested, known good die (KGD). This problem was exasperated by the fact that for EL technology there the voltages are high, and the power is significant.

FCOG: Flip-Chip-on-Glass technology consists of an IC driver that is bumped with gold or other metallurgy, and then electrically and mechanically bonded to mating conductor pads on the glass. The chip has to be designed specifically for the configuration of having the bumps down, in order to allow the input signal bus to address all IC's that share a side. The FCOG technology has the potential for the highest interconnect density of the technologies that have been mentioned thus far. Otherwise, the FCOG technology enjoys the same benefits and challenges as the COG technology.

## 2.2. Driving Forces of EL Interconnect

There are many factors that influence what interconnect technology is best for a particular display technology or display product. The major driving forces that determine which interconnect technology will be use on an EL display will be briefly discuss and how COG technology fits into this strategy. We have learned a great deal about the COG interconnect technology, its limitations and its strengths

as a result of designing and building two EL displays using COG. The driving forces for choosing an interconnect technology are summarized in Figure 1.

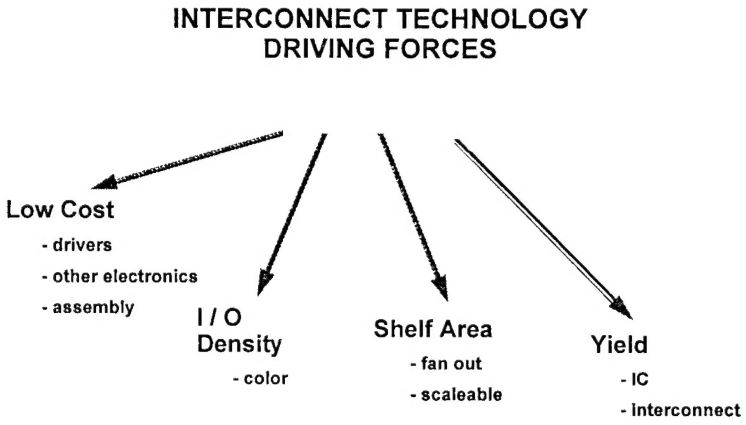



**Figure 1. Interconnect Technology Driving Forces.**

Interconnect Cost: The first driving force is the cost of the drivers. As shown in Figure 2, the cost of the drivers can be a significant portion of the total product cost. For this reason the choice of the interconnect technology is often decided solely on the cost per output I/O of the drivers. Other factors such as assembly time and capital equipment costs are also important. The estimated labor hours and the capacity of the COG pilot line is discussed in the equipment section of this report.

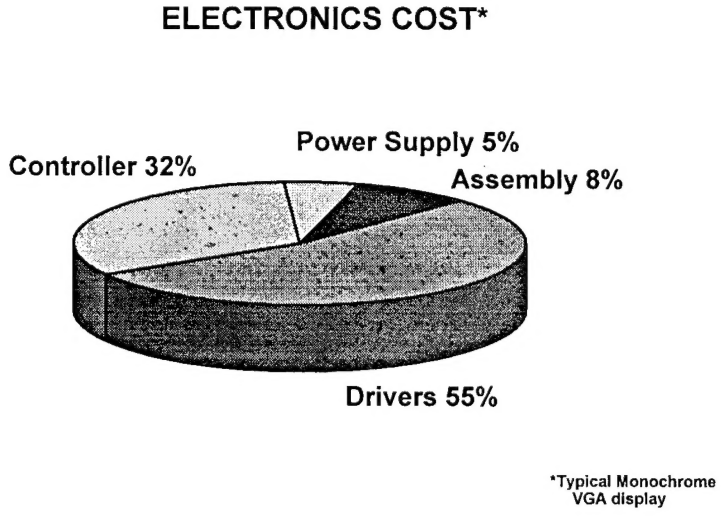



**Figure 2. Electronics Cost.** The relative cost of electronic components and assembly for TFEL displays.

Interconnect Density: In some cases the pitch requirements dictate the interconnect technology that must be used. For example, if less than 300um pitch is required, then the Elastomeric, the lead frame, and the HSC technologies would be eliminated from the possibilities, and the remaining technologies would be COG, TCP, or FCOG. The I/O density requirements of the new EL products, specifically the color displays, necessitate going to the finer pitches. The COG technology was demonstrated down to 120um pitch using 30um gold wire, and for Planar this was the practical limit. TCP and FCOG technologies will be uses for pitches less than 150um in the future. Figure 3 summarizes the ranges of I/O density for the TFEL displays.

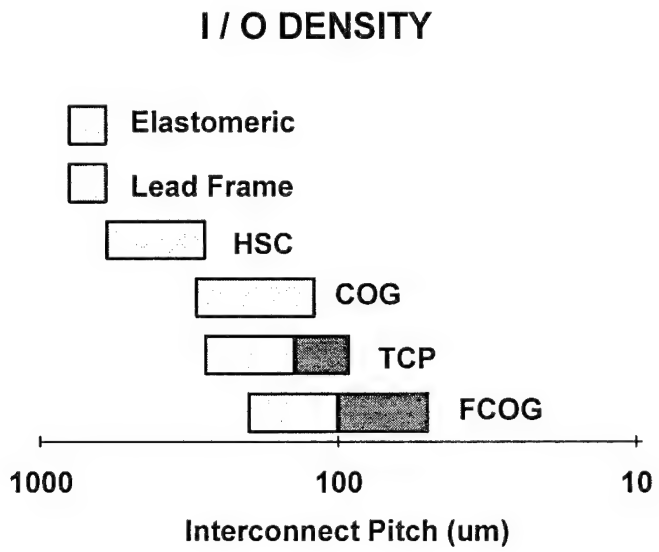



**Figure 3. I/O Density.** The lighter shaded areas indicate the range of pitches currently used at Planar, the dark shaded areas are strategic development.

Interconnect Yield: The EL display glass is burned in prior to the assembly of the product electronics, and current product is shipped with 100% functional pixels. The number of interconnects for various displays is shown in Figure 4. Planar's product has largely been in the range up to and including the monochrome VGA displays.

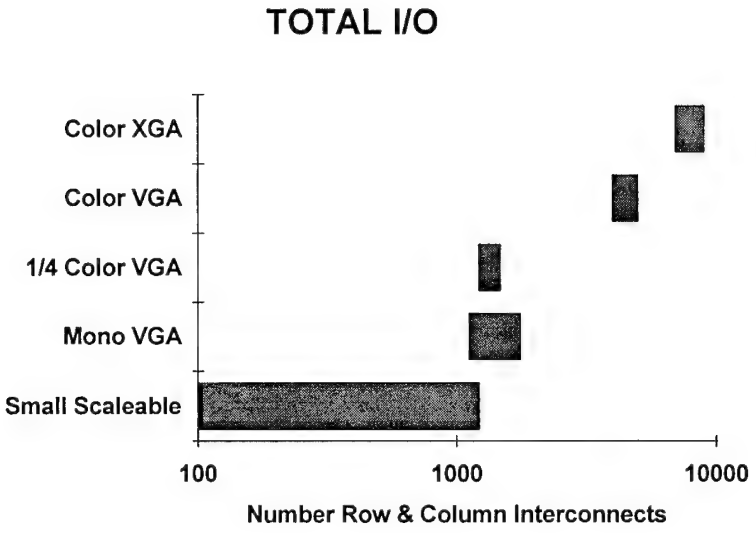



**Figure 4. Total I/O Demand.** The number of interconnects required for various display formats.

The first two displays that were assembled with COG technology as part of this SBIR program, were a split monochrome VGA and 1/4 VGA color display. The opportunities for error is proportional to the number of interconnects. The target per wire bond interconnect yield for the COG technology was under 100ppm. This target was not achieved and the per wire bond error rate was between 500ppm and 1000ppm. These errors were typically flame off errors as a result of a first or second bond not staying on the bond pad.

## 2.3. Strategic Interconnect Considerations

The various interconnect technologies have their strengths and weakness. The installation and debug of the COG pilot line brought to light some fundamental changes that are needed to optimize the COG process. The strategic interconnect activities specific to COG technology for EL displays are as follows:

- Higher temperature glass seal to allow higher temperature wire bonding. The maximum temperature for wire bonding the color display was reduced to under 110° C to ensure that the glass seal would not be degraded.
- Increased wireability, both escape and global in the top conductor layer to allow smaller shelf area. The shelf area on the two displays, that is the 1/4 VGA and the monochrome VGA, were made as small as possible, but still were not competitive with HSC, or Bent TCP shelf area.
- Lower resistance top conductor layer to prevent the voltage drop along the input signal and power bus. This voltage drop becomes significant with the larger displays.

- Back plate to front plate interconnect to allow putting the driver IC's on the back of the display. EL technology does not require a back light, so the back plate can be populated with electronic components and circuitry. What is needed is to have an interconnect method to connect the back plate to the front plate.

# 3. Equipment

## 3.1. Summary

The equipment used to assemble IC drivers to EL displays with wire bonding technology was typical hybrid assembly equipment. A brief description of the equipment is given, and also a description of any equipment modifications that were necessary for the processing of the panels. Both the die bonder and the wire bonder had to be modified to accept the displays that were significantly larger than the standard Hybrid, MCM, or other typical wire bond application. Photographs of the equipment are in Appendix A. The following list shows the major pieces of equipment that were purchased or built by Planar.

| | |
|---|---|
| Die Bonder | Hughes 2500-II |
| Epoxy Cure | Blue-M Convection Oven |
| Wire Bonder | Hughes 2460-III |
| Encapsulation | Asymtek A402-G |
| First Test station | Built by Planar |
| Pull Tester | Dage BT-14 |
| Shear Tester | Dage BT-24 |

## 3.2. Die Attach

The Hughes 2500-II die bonder is a general purpose die attach machine that is used extensively in the hybrid industry. Most of the hybrid assembly suppliers in the greater Portland, Oregon area used the Hughes 2500-II. Our used bonder was bought from Hughes directly, and was then modified for use with the EL glass and the EL driver IC's. The significant modifications to the machine are listed here.

Stage Modification: The Hughes 2500-II was equipped with an X-Y stage with a 5 x 12 inch travel. One of the first target applications to use the wire bonding was the VGA display that has dimensions of about 171mm x 221mm (8.7 x 6.7 inches). Therefore a stage was designed and built that allowed one side of the display to be populated with IC's, and then the stage is rotated to allow the other half of the display to be reached. Photograph A3 (in Appendix A) shows the modified stage.

Pickup Tool Modification: The driver IC's that were used for these initial applications were the HV72 and the HV621. Both of these die have a very visually repetitive top surface. Also, the size of the IC is large enough, and the placement

accuracy requirements were +/- 250um, so the die pick had to be as accurate as possible. After significant experimentation, the best location to sight the die with the pattern recognition system was along one edge of the die. Therefore, a pick up tool was designed and built that allowed sighting along the edge of the die while still picking the die up in the center. Photograph A3 shows the modified pickup tool.

Substrate Camera Modification: The second camera, which is the one that sights the glass substrate from on top, needed to have the lighting upgraded from the standard ring light. A through-the-lens light was installed because the thin film gold on the glass panels is too reflective for the standard diffuse lighting on the machine. Therefore a co-axial light source was added to the substrate camera. The capacity and unit hours for the Hughes die bonder is estimated for the FC2 display as follows.

**Hughes 2500-II**
**Throughput Calculations (FC2)**

| DIE ATTACH | | | | |
|---|---|---|---|---|
| Base Capacity | 3000 | daubs/hour | 303.80 | sec/panel |
| | 4 | daubs/die | | |
| | 31 | die/panel | | |
| | 5 | sec/die placement | | |
| Load-unload panel | 120 | sec/panel | 120.00 | sec/panel |
| Switch epoxy pot | 20 | sec/panel | 20.00 | sec/panel |
| Change tray & magazine | 10 | sec/tray | 9.60 | sec/panel |
| | 42 | die/tray | | |
| | 15 | sec/mag | | |
| | 5 | trays/mag | | |
| Load program | 300 | sec/program change | 3.00 | sec/panel |
| | 100 | panels/program change | | |
| Load epoxy pot | 600 | sec/8 hour shift | 0.85 | efficiency |
| Clean epoxy pot | 500 | sec/8 hour shift | 0.85 | efficiency |
| Number of operators | 1 | | | |
| Percent recycle | 1.15 | | | |
| Machine efficiency | 0.93 | | | |
| Operator efficiency | 0.83 | | | |
| Machine availability | 0.9 | | | |
| Die attach unit hour | 0.2614 | operator hours | | |
| **Die attach capacity** | **3.44** | **panels/hour** | | |

The IC's that have been placed in the epoxy with the die attach machine are then put into a curing oven. The oven used is a Blue-M atmospheric convection oven.

## 3.3. Wire Bonding

A Hughes 2460-II wire bonder was purchased from a local business that was in liquidation. The bonder was intended for initial process development, building prototypes, and display rework/repair. The venders considered for the pilot production bonder were MEI, Hughes, K&S, and Alphasem. After studying the

options, we decided to upgrade the Hughes 2460-II to a Hughes 2460-III. The upgrades included, new camera and optics, digital control servos, higher resolution encoders, 5"x12" table travel, new transducer and z-axis assembly, and upgraded software. With the upgrade, the wire bonder was ready for medium volume assembly and to be used as the primary manufacturing tool, as well as for rework.

Stage Modification:

A large heater stage was designed for the Hughes wire bonder. The large heater stage is required for the bonding of the SBIR VGA display, which is 8.7 x 6.7 inches. A stage was designed and built that met the weight, flatness, and temperature uniformity requirements, but produced inconsistent bonds due to ringing vibration during while decelerating the table. The acceleration and deceleration profiles were changed to try to stop the ringing, but this was not successful. The stage was reworked to be stiffer and lighter, but when tested it still produced inconsistent bonds due to the unwanted vibration. Finally, an over sized heater stage (4" x 6") was ordered from Hughes and was modified to accommodate the VGA panel. The oversized heater stage also has mass of about 4.7Kg. The temperature was not as uniform as that of the custom designed stage, but the ringing was eliminated by decreasing the acceleration and deceleration profiles on the XY table. The heater stage required heat reflectors because it radiates significant amount of heat when the temperature is set at 140° C. The maximum stage temperature range was 7° C from hottest to coolest. In the bonding area the range was 4° C. The temperature uniformity was improved by modifying the heater stage circuitry to allow for greater power to be delivered to the heater cartridges. The temperature control circuit is now wired separately for the power circuits, and the heater cartridges are wired in parallel instead of in series.

The largest panel dimension that was to be bonded on the Hughes 2460-III was 171mm x 221mm (8.7 x 6.7 inches). In order to get bonds on all sides of the glass panel, the tooling plate on top of the heater stage was built large enough for the glass, but was mounted off set towards the front of the machine. The largest panel had to be assembled by running two separate programs. The first program could wire bond the entire length of the panels and approximately 5 inches of the width. The panel was then rotated 180 degrees (while still hot), and the second program would be run to bond the remaining driver IC's to the display.

Additional work on the wire bonder included the installation of an upgraded EFO (electronic-flame-off) wand and a different style transducer. Both of these changes to the wire bonder have provided much more consistent bonds and we are bonding at an error rate of 500 to 1000ppm per wire. The throughput and capacity of the wire bonding operation was estimated as follows for the FC2 display.

**Hughes 22460-III**
**Throughput Calculations (FC2)**

**WIRE BOND**

| | | | | |
|---|---|---|---|---|
| Base capacity | 2 | wires/sec | 1302 | sec/panel |
| | 84 | wires/die | | |
| | 31 | die/panel | | |
| Wire set up | 600 | sec/spool | 130.2 | sec/panel |
| | 1200 | in/spool | | |
| | 0.1 | in/wire | | |
| Load Program | 300 | sec/program change | 3 | sec/panel |
| | 100 | panels/program change | | |
| External handling | 120 | sec/panel (load-unload) | 120 | sec/panel |
| Number of operators | 1 | | | |
| Percent recycle | 1.15 | | | |
| Machine efficiency | 0.93 | | | |
| Operator efficiency | 0.83 | | | |
| Machine availability | 0.9 | | | |
| Wire bond unit hour | 0.6436 | operator hours | | |
| **Wire bond capacity** | **1.40** | **panels/hr** | | |

## 3.4. Cable Bonder

Cables were attached to the glass panel using an existing piece of Planar equipment that is used for bonding TCP to glass with anisotropic Adhesive Film (ACF). The cable flex material was made out of polyimide and was bonding to the glass with the same process and equipment as we use to bond TCP to glass.

## 3.5. Encapsulation

The Asymtek A402G machine was purchased to dispense the material that is used to encapsulate the wire bonds and the thin film metals. The encapsulation provides electrical isolation, corrosion resistance, and mechanical protection. The Asymtek machine can be programmed to dispense at different rates and in complicated geometry. Two encapsulation materials are used with COG technology. The first material is put down as a thin bead that defines the area to be covered by forming a dam, and it retains its shape as applied. The second material fills in the area that was defined by the dam material. One modification was made to the Asymtek machine to allow for both materials to be dispensed during the same process step. The modification was to add the dual toggle head assembly.

Dual Toggle Head modification: A dual toggle head was installed on the Asymtek machine so that the dam and filler material could be dispensed during the same process step. The two heads were a known offset apart, and so the program was written to build the dam with one material, and then fill the dam with the second material. Photograph A5 shows the dual toggle head assemble. The displays were then put into a convection oven to cure both dam and filler material at the same time. The throughput and capacity of the Asymtek encapsulation machine was estimated as follows for the FC2 display.

**Asymtek A402G**
**Throughput Calculations (FC2)**

**ENCAPSULATION**

| | | | |
|---|---|---|---|
| Base capacity | 10 | sec/dam | 120 sec/panel |
| | 4 | dams/panel | |
| | 20 | sec/fill | |
| | 4 | fills/panel | |
| | 31 | die/panel | |
| Load-unload panel | 120 | sec/panel | 120 sec/panel |
| Load program | 300 | sec/program | 60 sec/panel |
| | 5 | panels/program | |
| Load dam material | 300 | sec/load | 60 sec/panel |
| | 20 | dams/load | |
| Load fill material | 60 | sec/load | 2.4 sec/panel |
| | 100 | fills/load | |
| Number of operators | 1 | | |
| Percent recycle | 1.05 | | |
| Machine efficiency | 0.97 | | |
| Operator efficiency | 0.83 | | |
| Machine availability | 0.9 | | |
| Encapsulation unit hour | 0.1313 | operator hours | |
| **Encapsulation capacity** | **6.86** | **panels/hour** | |

## 3.6. Pull & Shear Testing

The Dage BT-14 pull tester and the Dage BT-24 shear tester were the primary feedback method for the process. The pull tester was used to check the strength of the stitch or second bond, and the shear tester was used to optimize the gold ball bond or first bond. A precision vacuum stage was designed and built for the BT-14 to hold the glass while pull testing. Photograph A6 shows the BT-14 with fixture, and Photograph A7 shows the BT-24.

## 3.7. Rework

The rework of COG glass required no new equipment. The tools used were a scalpel, and a soldering iron with the appropriate size tip. The wire bond operation was then done with the same equipment that was used for initial assembly. The die attach and encapsulation process step were done manually.

The throughput and capacity of the rework operation was estimated as follows for the FC2 display.

## Rework
## Throughput Calculations (FC2)

**REWORK**

| | | | | |
|---|---|---|---|---|
| Base capacity | 600 | sec/die before encapsulation | | |
| | 1200 | sec/die after encapsulation | | |
| | 31 | die/panel | | |
| Percent rework before encapsulation | 0.02 | | 12 | sec/every die |
| Percent rework after encapsulation | 0.01 | | 12 | sec/every die |
| Rework Unit hour | 0.2067 | operator hours | | |
| **Rework Capacity** | **N/A** | | | |

## 3.8. Material Handling

Several unique tools have been developed for the handling of the glass panels during the die attach and wire bonding processes. First, the color panels are being transported from glass manufacturing to electronic assembly in protective carriers. The protective carriers are also used to store the panels in-between process steps during electronic assembly.

Another unique tool was developed to load and unload the panels in the assembly machines. This tool is a vacuum puck made out of nylon, as shown in Photograph A11. It is used to pick up the panel from the various machines without excessive handling. The pucks can be used two at a time to turn a panel over, as is necessary with the color panel. There are sets of two at the die attach machine, the wire bonder, the encapsulation machine, the shear and pull testers, and several more sets will be installed as needed at the curing ovens. The manual material handling causes occasional damage even with the aid of the unique tools.

## 3.9. Facilities

The original plans called for a class 10K clean room of approximately 400 square feet. After the equipment was installed and debugged it was determined that laminar flow hoods over the wire bonder and die bonders would be enough for all the process development work and limited production. These were installed and can be seen in Photograph A1 over the Hughes 2500-II and the Hughes 2460-III.

# 4. Process Development

## 4.1. Introduction

Planar visited several companies involved in chip on glass development. Planar visited Interpoint in Redmond WA, for a vendor survey. Interpoint specializes in providing chip on glass and chip and wire processing and product to the hybrid industry; and they are being used as a supplier for another COG project at Planar. Interpoint provided valuable process information including chip on glass design rules for layout of the driver chip fan out and bond pads. Planar also visited Plasmaco in Highland, NY. Plasmaco has been manufacturing AC plasma displays for several years using COG technology for the driver interconnection to the display panel. We were able to observe panel production using chip on glass.

## 4.2. Process Flow

The COG technology process flow for the EL display assembly is significantly different from the normal glass assembly using either Elastomeric, or lead frame interconnect technology. Specialized equipment is required for COG assembly. The die attach, the wire bonder, and the pull & shear testers were new to Planar and required training for engineering, maintenance and operation. The COG process also required a cleaner work area, and flow hoods were installed to help keep debris off of the bond sites. Another significant change over the standard assembly process for EL panels was the handling of panels with several thousand delicate wires during the several steps in the process. The process flow is shown in the Figure 5. below. Each of the process steps will be described in detail in the sections that follow.

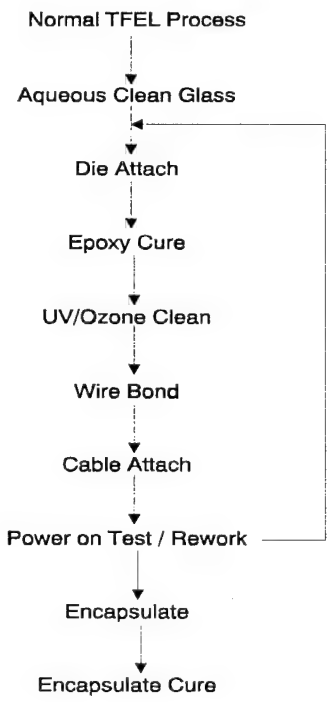



**Figure 5. COG Process Flow.**

## 4.3. Process Steps

### 4.3.1. Die Attach

The Hughes 2500-II die-bonder uses pattern recognition (PR) to pick up the die from waffle packs. The PR was characterized using the HV621 column drivers and a standard piece of Planar glass with thin film metals. An experiment was performed that consisted of sighting fiducials on the glass then placing the HV621 die onto a strip of closed cell urethane foam that was positioned next to the glass. The die placement accuracy and repeatability was then measure from the fiducials. The die were placed with five different pickup accuracy's during five separate machine set ups. The results showed that the die-bonder is capable of placing die with a repeatability of +/-250um at a 4.5 sigma quality level when set up with the highest pickup accuracy. The higher pickup accuracy settings tended to slow the base machine cycle down.

Die attach epoxy: On the first FC2 the driver IC's were hand placed and attached with a UV curable adhesive (Loctite 352). We then evaluated two thermally cured die attach epoxies. Both epoxies are made by EPOTEK, one is the H31D, and the other is H61. Both epoxies are used extensively in the MCM and Hybrid industries. The cure schedule for these epoxies allowed us to keep the temperatures low enough to not effect the glass seal. The evaluation determined what parameters

were required to remove and replace a driver IC on a glass panel. The results showed that these thermally cured epoxies allowed for repair of die on the panel with little risk of damaging the panel.

### 4.3.2. Wire Bonding

The Hughes (2460-III) ball bonder was initially set up with an over sized heater stage to accommodate the monochrome VGA display. The XY table servo motors were slowed down to 25% of full acceleration and deceleration to ensure that the table would be settled out before the bonding started.

Bonding pads: The ball bond pads on the HV621, HV72, and HV70 are 100um by 100um. The IC pad metallurgy is 99% Al and 1% Silicon with a thickness of 30um. The initial work showed that the stitch pads on the glass must be at least 430um long to allow for two rework cycles when required. The stitch pads have been made as wide as possible by using two interstitial rows. The row closest to the die has stitch pads that are 190um wide, and the row closest to the active area of the glass has stitch pads that are 100um wide. We determined that bottle neck capillaries were not required for the 120um pitch because we used a mirrored interstitial footprint design (see the design section).

Gold wire: Two wire sizes were ordered for the design matrix, 30um and 25um in diameter. The wire elongation values were 2% and 8%. After the initial screening experiments, all on the remaining process optimization experiments used the 30um wire, with 8% elongation. The 30um wire was required to reduce the sagging of the wires on the long runs to relatively small pads. There was no measurable difference between the 2% and 8% elongation wire, and the 8% elongation wire was chosen because it was recommended by the manufacturer of the wire bonding equipment.

Bonding capillaries: Samples of capillaries were ordered with various tip diameters, face angles, and hole diameters. The face angle that were used in the initial screening experiments were 4° and 11° face angle. The tip diameters and hole diameters were ordered to match the 25um and the 30um diameter wire. The process optimization experiments were performed using a capillary with a face angle of 11°, and a tip diameter was standard for 30um wire. The hole diameter used for process optimization was larger than normally used for 30um wire. The larger hole diameter gave less loop control on the wire, but it eliminated the clogging that we experienced during the screening experiments. The trade off was necessary because thin film metal stack is relatively soft, and gold and aluminum would stick to the end of the capillary.

Process temperature: The process temperature for wire bonding EL panels kept below 120° C based on series of experiments performed on the back seal process.

This temperature is below the normal thermosonic ball bonding temperatures, but we were still able to get wide process windows.

Heater Stage Flatness: The oversized heater and stage had to be level to with in 150um over the 5 x 12 inch area.

Wire Bonding Process Optimization:
A wire bonding experiment was performed to establish the variable setting that gave reliable second bond shear strength. The control variables were capillary force, time, and power. The bond temperature was held constant at 130° C, which is the target bond temperature for the EL displays. The response variables were average pull strength, pull variance, average shear strength, shear variance, and number second bonds that pulled rather than broke. The wire was 30μm Au. Fifteen pulls or shears were averaged for each condition. A D-optimal experiment was used. The ranges for the control variables were as follows:

| | | | | |
|---|---|---|---|---|
| force | 75 | 85 | 95 | gf |
| time | 25 | 35 | 45 | ms |
| power | 75 | 85 | 95 | mW (current mode) |
| temperature | | | 130 | $^{\circ}$ C (constant) |

The temperature variations were monitored and were significant, that is up to -15$^{\circ}$ C less than the control set point. These variations indicated that the heater stage temperature control was inadequate and would have to be improved. The heater stage was modified at a later time, and the temperature variations have been eliminated.

The analysis showed that the power should be set at the high level and the time and the force should be set at the low levels. The first FC2 displays were built using the variable settings force=75gf, time=25ms, power=95mW, and the temperature=130$^{\circ}$ C. There were no problems with the glass seal, but later testing showed that statistically we would have problems with the seal if repeated rework cycles were required. The temperature was then lowered to a maximum of 120$^{\circ}$ C.

A second experiment was performed to investigate wire bonding to Planar EL glass panels at lower temperatures. The heater stage was modified by adding additional heater cartridges and running the heater cartridges in parallel for faster response time. A 25 trial D-optimal experiment was performed, similar to the one described previously. The differences were that HV621 die were used instead of bonding first and second bonds to glass. The temperature of the stage was an additional control variable. The control variables were capillary force, time, power, and temperature.

The response variables were average pull strength, pull variance, The wire was 30μm Au. The metal surface for this experiment was 500Å Cr, 10KÅ Al, 500Å Cr, 1000Å Pd, 1000Å Au metal stack. Five wire pulls were averaged for each trial condition, and were from the same side of each die. The ranges for the control variables were as follows:

| | | | | |
|---|---|---|---|---|
| force | 75 | 85 | 95 | gf |
| time | 25 | 35 | 45 | ms |
| power | 75 | 85 | 95 | mW (current mode) |
| temperature | 91 | 115 | 143 | °C (constant) |

The analysis showed that the second bond or "stitch bond" could be made at a lower temperature then previously assumed. The results are shown in Figure 6. At the same time, the shear strength of the first bond or "ball bond" was not significantly reduced with the lower temperatures. The average ball shear strength when bonded at 143° C was 67.5gf, and at 115° C the average ball shear strength was 65.7gf. The lower bonding temperature will be a benefit for through put and protecting the glass seal on the FC2 display.

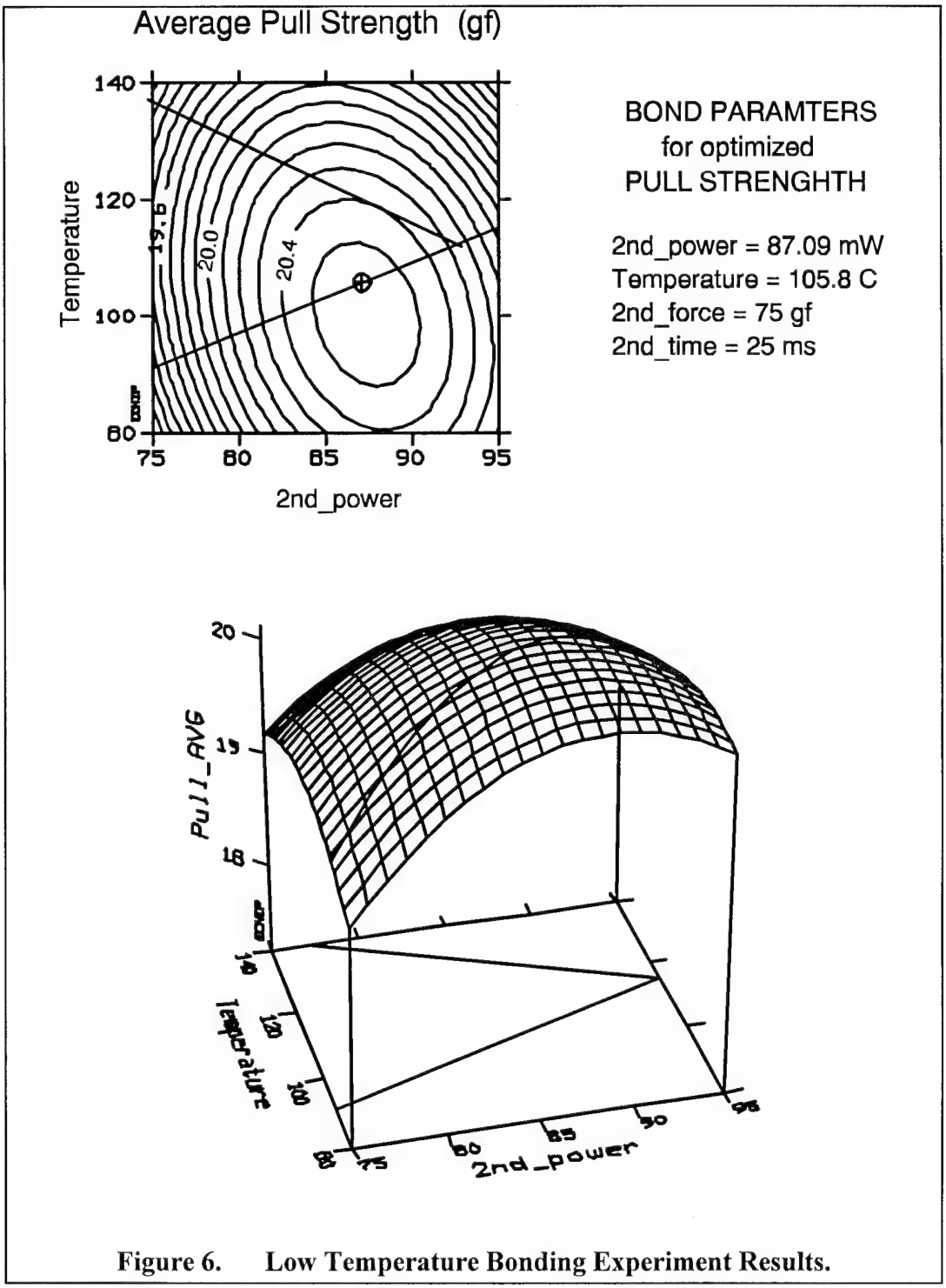



**Figure 6. Low Temperature Bonding Experiment Results.**

A third experiment was performed to look at the effect of the substrate metal softness on the wire bond parameters. We designed a 21 trial D-optimal experiment with 9 replicate trials. The Hughes wire bonder was programmed to

bond 10 wires for each trial for a total of 300 wires for each substrate metal stack type. The optimum bond parameters were determined for each substrate metal stack. The substrates used for this experiment were variations of the normal (Low-Z) thin film metal stack. The two experimental metal stacks are RC1 and RC2 and are shown in the table below, along with the standard Low-Z metal stack.

| Standard **Low-Z** | Experimental **RC1** | Experimental **RC2** |
|---|---|---|
| 500Å Cr | 1,000Å Cr | 500Å Cr |
| 10,000Å Al | 3,000Å Al | 3,000Å Al |
| 500Å Cr | 1,000Å Cr | 2,000Å Pd |
| 1,000Å Pd | 3,000Å Al | 3,000Å Al |
| 1,000Å Au | 2,000Å Pd | 2,000Å Pd |
| | 1,500Å Au | 1,500Å Au |

The bonds were made on the glass substrates with no die attached. The wire used was 30μm Au with 5-8% elongation. All of the bond pulls failed in the wire or at the stitch bond (second bond). No failures occurred at the ball bond (1st bond). The ten wires were pulled and the pull forces were averaged for each trial condition. The ranges for the control variables were as follows:

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| force | 50 | 67 | 75 | 83 | 100 | gf | |
| time | 20 | 30 | 35 | 40 | 50 | ms | |
| power | 50 | 67 | 75 | 83 | 100 | mW | (current mode) |
| temperature | | | | | 110 | °C | (constant) |

The experiment confirmed that the softer metal stack, that is RC2, required lower force and power settings for optimal bond pull strength. However, both metal stacks gave acceptable bond pull strengths and the metal stack will be determined by cost and electrical performance. The response surface of the results of the experiment are shown in Figure 7.

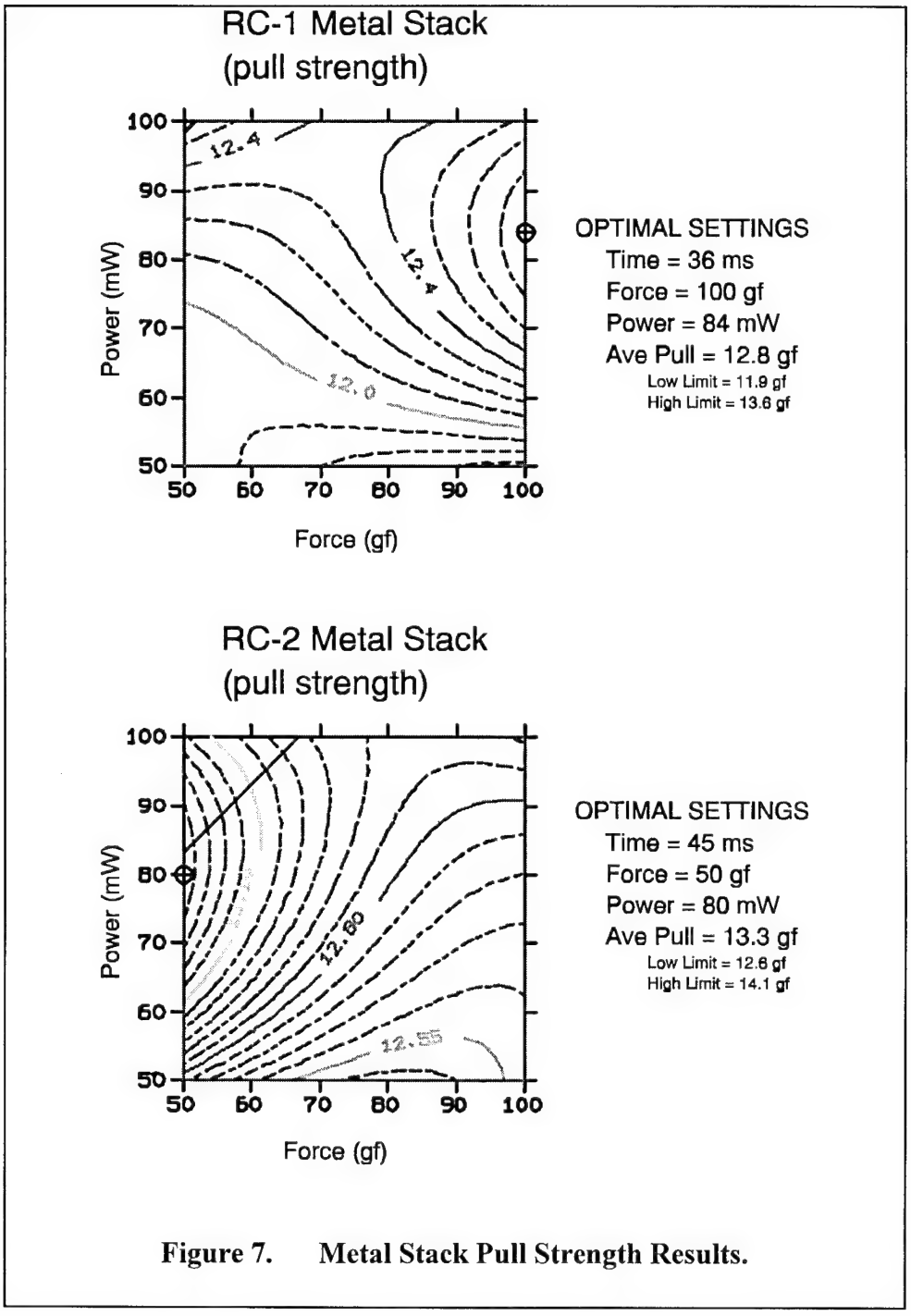



**Figure 7. Metal Stack Pull Strength Results.**

### 4.3.3. Rework

A rework and repair procedure for the prototype displays was developed. The constraint on the rework process was that the rework site temperature should stay

below 150° C for the short period of time for chip removal. Care must be taken to avoid touching the adjacent components and wire bonds. The IC's were removed by hand with a custom solder iron tip and about 8oz of pressure. When the chip conducted enough heat to the epoxy, it softened and the chip slid off the glass. A new die was attached by hand, cured, and then cleaned in the UV/$O_3$ cleaner. The IC's were then wire bonded and retested. Well over 200 electrically bad column and row drivers have been removed and replaced on the FC2 displays using this process.

#### 4.3.4. Encapsulation

The thin film metallurgy on the glass needed to be isolated because of the high voltages. The encapsulation also served to mechanically protect the wire bonds. GE RTV 655 silicone encapsulate was used initially. We did not use primer so that rework of the chip after encapsulation might be possible. The adhesion was not adequate, and if the panels were handled the encapsulate would lift at the edges. Therefore, we started using GE 4120 RTV primer for glass. The primer made rework of an IC very difficult if not impossible after encapsulation.

We also evaluated the GE 656 encapsulation. It is very similar to the GE 655 that we are currently using, but it is not recommended for use where the temperature drops below -60° C. The GE 655 has a useful temperature range of -115° C to 204° C.

### 4.4. Yield

#### 4.4.1. Driver IC's

The Known-Good-Die (KGD) problem was severe for the SBIR display. There were several reasons for the problem.

- The HV621 column driver was a newly developed driver
- This was the first time that the drivers were used as bare die
- The testing methodology at the IC supplier was in development stages, and therefore the die were not fully tested, and excessive probe marks were found on the IC bond pads.

The summary of the data collected during the pilot line build is shown in table below. The number of driver IC's per display is 31, of which 16 are HV72 row drivers and 15 are HV621 column drivers. The blue substrate has 8 row drivers and 5 column drivers. the Red/Green substrate has 8 row drivers and 10 column drivers. The following is a summary of the first pass yield of the FC2 product.

Driver IC Yield

| | Blue Substrate | | Red/Green Substrate | |
|---|---|---|---|---|
| | Row (HV72) | Column (HV621) | Row (HV72) | Column (HV621) |
| Fraction Fail | 11 of 344 | 20 of 215 | 2 of 344 | 17 of 430 |
| Percent Yield | 96.8% | 90.7% | 99.4% | 96.0% |

The yield was also looked at by display panel, and rows versus columns. The row drivers had a higher yield at first turn on than did the column drivers, which was contrary to initial expectations. The blue substrate had a lower driver yield at first turn on than did the Red/Green panel, which was expected because of the significantly higher capacitance of the blue substrate. The blue substrate is about double the power consumption of the Red/Green substrate.

Driver IC First Pass Yield
(by location on panel)

| | Row | Column | Combined |
|---|---|---|---|
| Blue | 98.6% | 90.7% | 94.5% |
| Red/Green | 99.4% | 96.0% | 97.5% |
| Combined | 98.1% | 94.3% | |

The yield of the panels at first turn on was unacceptably low due to the driver IC failures. The weighted average yield of the drivers at first turn on was 96.2%, and the expected display yield would be 0.968^8 x 0.907^5 x 0.994^8 x 0.96^10 = .301, and the actual display yield was 34.9% as shown below.

| | Display Yield |
|---|---|
| Fraction Display Fail | 28 of 43 |
| Percent Display Yield | 34.9% |

The theoretical curves for the number of drivers versus display yield is shown in the Figure 8. The vertical line at 31 driver IC's indicates the penalty for having 96.2% yield on the drivers.

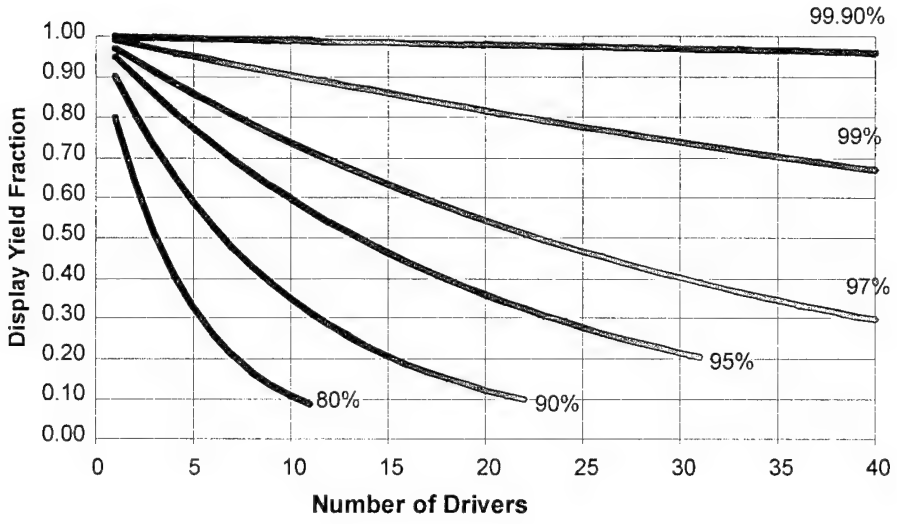



**Figure 8. Driver Yield.** The effect of driver yield on the display yield.

### 4.4.2. Wire Bonding Yield

The expected display yield due to wire bond defects is shown in Figure 9 and is estimated by the experimental runs while setting up the bond parameters. The number of wire bonds on the FC2 display is 1903, The number of wires on the monochrome VGA display is 2320.

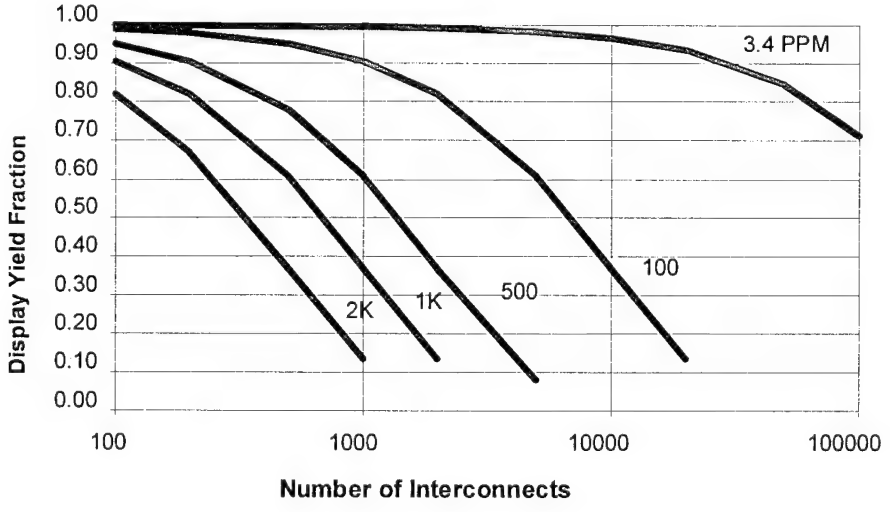



**Figure 9. Interconnect Defects.** The effect of interconnect errors on display yield.

### 4.4.3. Yield Conclusions

The first pass yield of the bare die driver IC's for this project averaged 96.2%. For a display application, such as the EL320.256 display, which requires 32 driver IC's, the theorectical first pass display yield would be about 29%. A yield this low is unacceptable for EL displays. The driver IC yield would need to be at least 99.7% for a display with 32 driver IC's to meet the commercially viable 90% first pass display yield.

The first pass yield of driver IC's of 96.2% would be acceptable for displays with up to 2 driver IC's.

## 5. Design Layout Guide

### 5.1. Glass Design

The wires coming from the output side of the HV621 column driver are on the tight pitch of 120um, and therefore many pad layout designs have been studied to come up with the optimum design for this EL application of COG. The first pass "optimized" footprint has the wires leaving the driver in an alternating fashion, with first a short wire, and then a long wire. These wires will terminate on the glass stitch pads that are a mirror image of the die pads. The long wires are designed to be higher off the plane of the glass, and therefore be less susceptible to touching the next nearest neighbor that is a short wire and that has been designed to be closer to the plane of the glass. The interstitial arrangement gives the effect of doubling the pitch to 240um for some of the variables like wire pitch.

The design ground rules that were established as a result of these displays being designed and built with wire bonded IC's are summarized in the following layout design statements.

Clearance areas: The IC's must have a clear area of +/- 250um around the entire perimeter to allow for die bonding tolerances as shown in Figure 10.

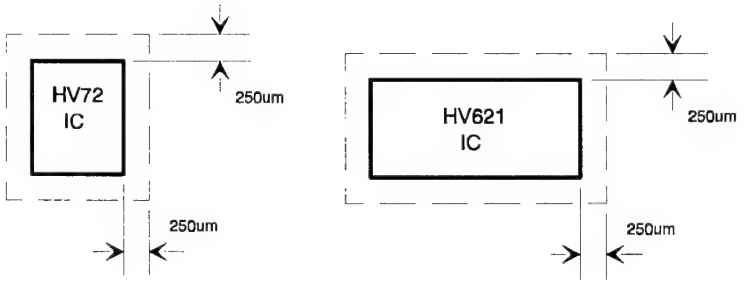



**Figure 10. Clear Area Around IC's.**

Minimum pad dimensions: The minimum pad dimensions for the second bond is 100um by 430um. The preferred dimensions are at least 150um by at least 430um. These dimensions give enough room to rework the die twice. If more rework is anticipated then the length of the pads should be increased by 150um for each additional rework. The increased length should be away from the IC as shown in Figure 11.

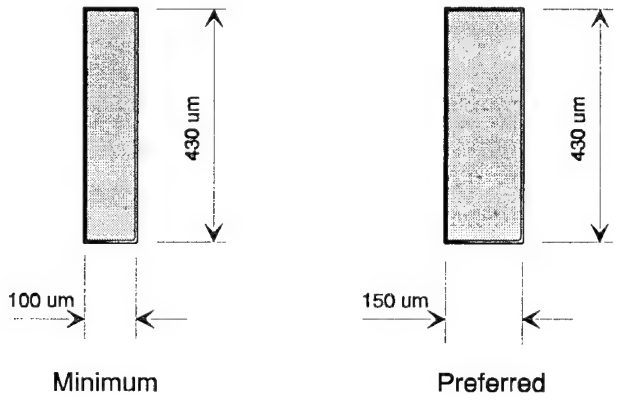



**Figure 11. Second Bond Pad Size.**

Min/Max line length: The minimum bonded length is 1200um for the 30um gold wire and the maximum length is 3000um as shown in Figure12. The maximum length is determined by the amount of acceptable sagging under the weight of the wire. When the wire is too long, the sagging of the wire cause the wire to approach the glass bond pad at a shallow angle and tends to short adjacent bus lines that are running perpendicular to the wire. Also, the longer wires are less determinant and less repeatable, hence tend to short between adjacent wires.

The minimum length is determined by the loop geometry as it is coming off the IC and assumes worst case IC placement tolerance, that is that the IC is off in the direction of the glass bond pad which has the effect of shortening the wire length by 250um. The failure mechanism when the wire length is too short is that the wire touches the edge of the IC and causes an electrical short between the edge of the IC and the wire.

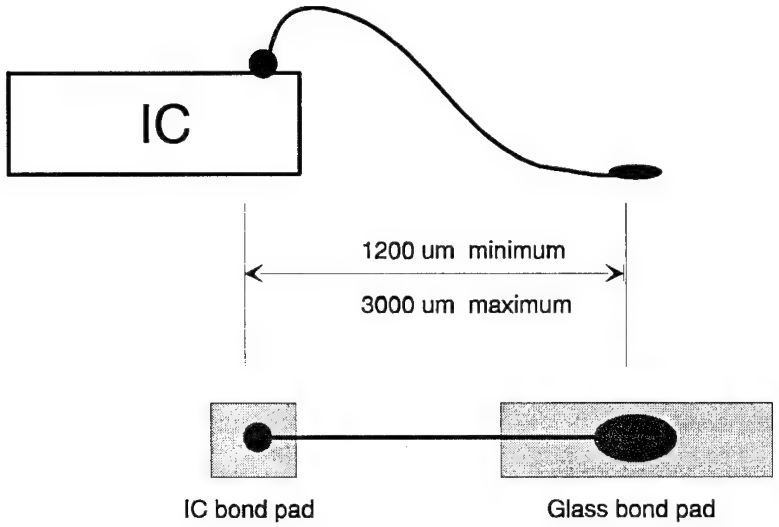



**Figure 12. Wire Length Recommendations.**

Die to die spacing: The IC to IC spacing is determined by the ability to rework. There are two cases for minimum spacing as shown in Figure 13 and Figure 14. The first is when there are no wire bonds in the area between two components. In this case the spacing is limited by the IC placement accuracy and the ability to remove an IC during a rework operation without effecting the adjacent IC.

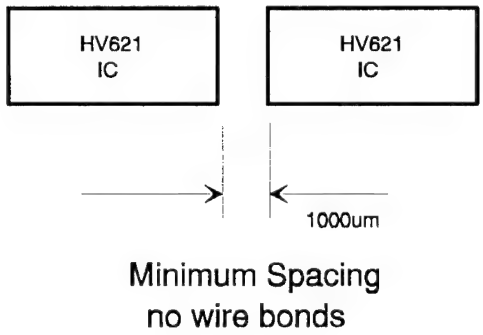



**Figure 13. Column Driver Minimum Space.**

The second case that is considered is when there are wire bonds in the area adjacent to two IC's. In this case the minimum spacing is increased in addition to the first case by the amount needed for wiring on the glass and the additional fragility of the wires.

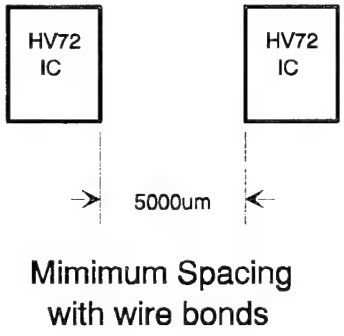



**Figure 14. Minimum Space for Row Drivers.**

Minimum pitch: The minimum effective wiring bonding pitch is 120um when the layout is staggered as shown in Figure 15. The wire use is 30um diameter gold wire. When the pitch is not staggered, the minimum pitch is 200um.

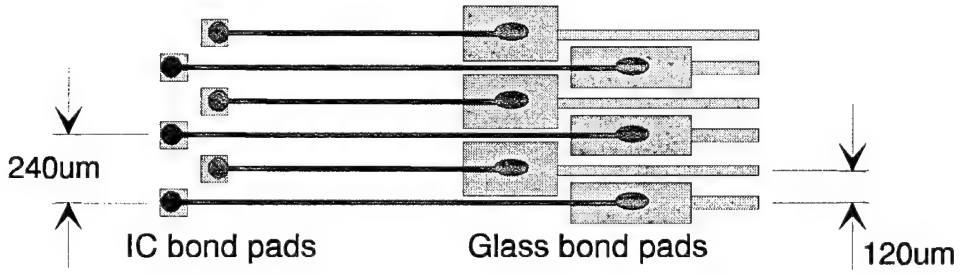



**Figure 15. Minimum Pitch for HV621 Column Driver IC's.**

The design for the column shelf area of the monochrome VGA display is shown as a cross section in Figure 16. The amount of space on the edge for input power and ground was not enough as there was significant voltage drop due to the resistance of the thin films and the high voltage that is used to drive the EL displays.

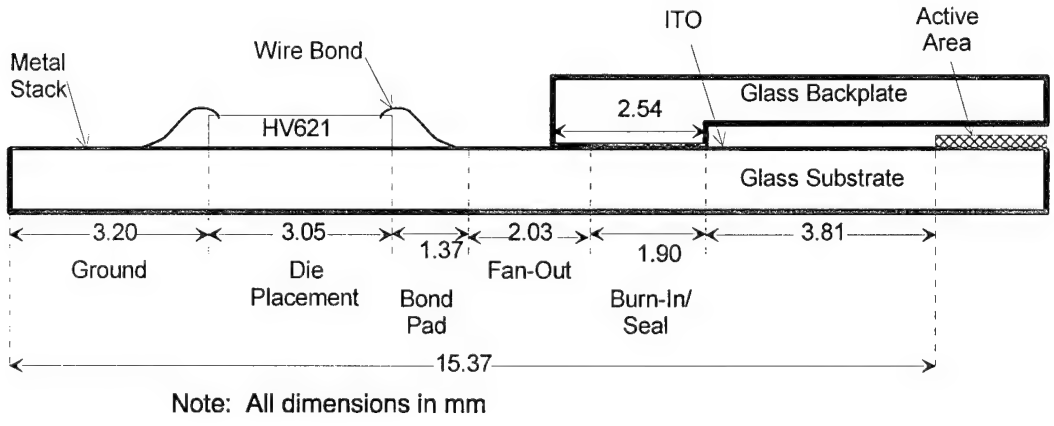



**Figure 16. Column Shelf Area on the Monochrome VGA Display.**

## 6. Electrical Design

### 6.1. Drive Method

A gray scale drive approach was chosen for the COG display developments. This approach was based upon a low cost, pulse width modulating technique. Sixteen gray levels were obtained, with reduced power and increased brightness compared to previous TFEL gray scale displays. Driver cost was reduced with the use of a new 2-bit column driver.

To demonstrate this gray scale approach using COG drivers a monochrome VGA display was developed. This display used optimized existing gray scale techniques, a split column panel architecture, and a new column driver. Regarding color COG displays, a 320.256 display was the display selected to use this packaging approach.

It was possible to achieve 16 gray levels using a 2-bit (4 level) column driver by incorporating 2-frame averaging. During the first frame the pixel is driven to one of four levels, and during the second frame the pixel is driven to one of a different set of four levels. The resulting overall brightness is the average of these two levels. By carefully selecting the appropriate levels it is possible to get 16 separate, monotonic levels. This is shown in the Figure 17.

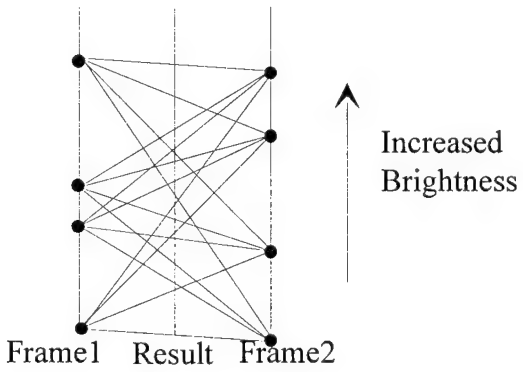



**Figure 17. Gray Scale Monotonic Levels.**

Gray scale levels are monotonic and approximately linear as the measured data in Figure 18 shows.

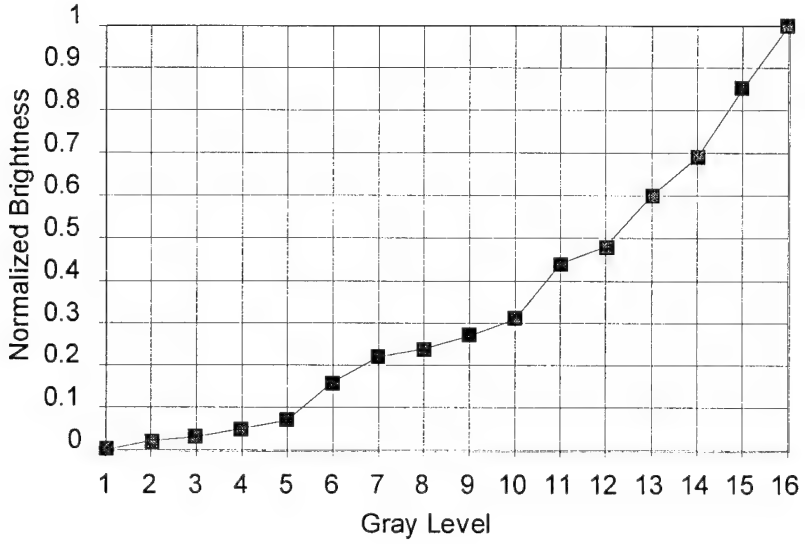



**Figure 18. Gray Scale from Pulse Width Modulation.**

Undesirable display artifacts, such as shadowing (changing brightness along a row a column versus loading) were minimal and reduced compared to the previous TFEL displays.

## 6.2. Column Drivers

Requirements

The basic requirements for the column driver are; 1) accommodate an output interconnect pitch of 150 microns, and 2) allow a method for adjusting pixel brightness independently. The HV621, a new pulse width modulating, TFEL gray scale driver was developed for this purpose.

Results

Two primary problems needed to be solved in order to reliably use this driver for COG displays. In summary these problems were;

1) Prevent latchup due to large voltage transients on the power traces on the glass. This problem was minimized by adding extra wire bonds along the critical power traces. While this approach was suitable for small displays of approximately 6" diagonal or less, the problem remained on larger panels using pulse width modulation as the drive approach. It was not possible to reliably operate a large panel without disabling the PWM operating mode in order to significantly reduce the current transients in the power traces.

2) Performance problems with the die. Planar engineering worked with the vendor (Supertex) to resolve design and testing problems. Problem resolution was difficult because the driver could not be placed in a package that would aid high speed testing. Furthermore the vendor did not have high speed test

capability at the die level, and therefore they initiated a program to install this capability. Because of these issues there is the need to replace bad die at first turn-on of the displays.

## 6.3. Row Driver

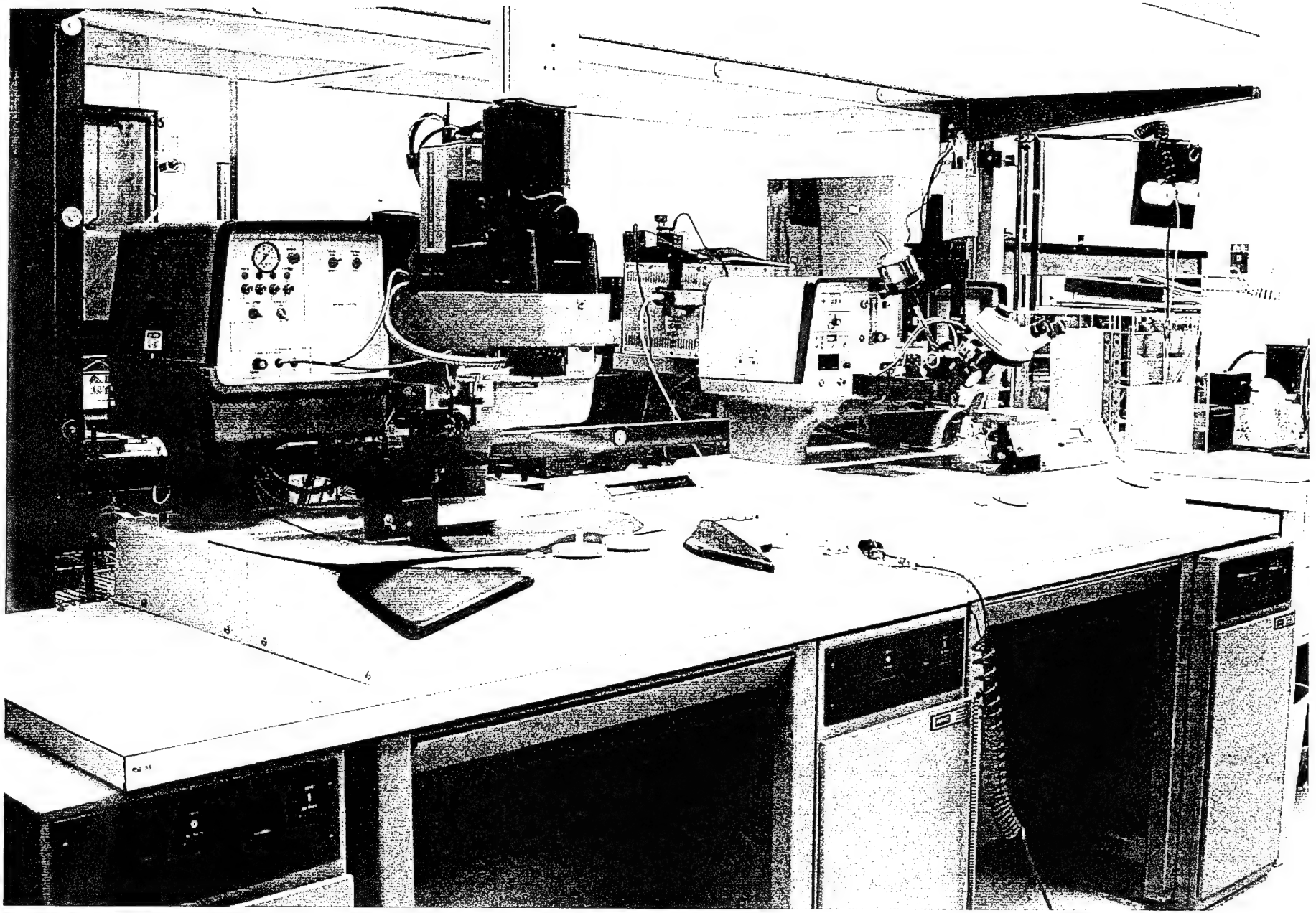
Requirements

A row driver capable of driving a single row of a split column panel was required. For small color displays a 34 output DMOS row driver from Supertex (HV70) was used, as it was the only row driver available in die form at the time. For the large VGA panel, a 40 output DMOS row driver from Supertex (HV72) was used.

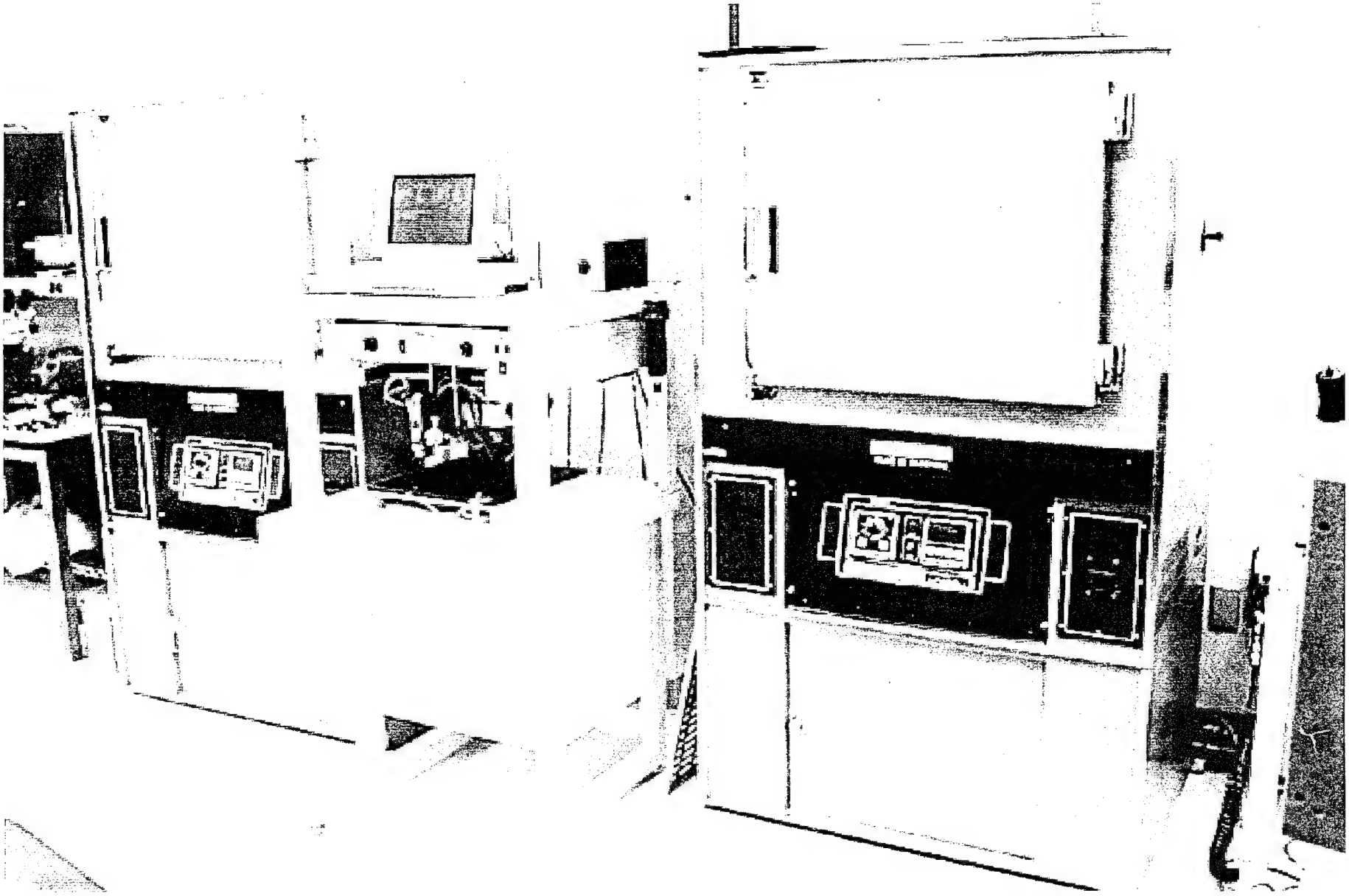
Results

There have been significant reliability issues using these row drivers for high performance color and monochrome displays in a COG environment. Since the drivers will fail if the output current specification is exceeded, there were very stringent requirements on the wire bond integrity, controller operation, and test coverage of the die. In summary, all conditions had to initially be correct and remain that way during operation or a row driver failure would occur. While it was reasonable to meet these conditions for smaller monochrome displays, it was not possible to achieve reliable operation on color or large area monochrome displays. This requires a large amount of rework for these more demanding displays.

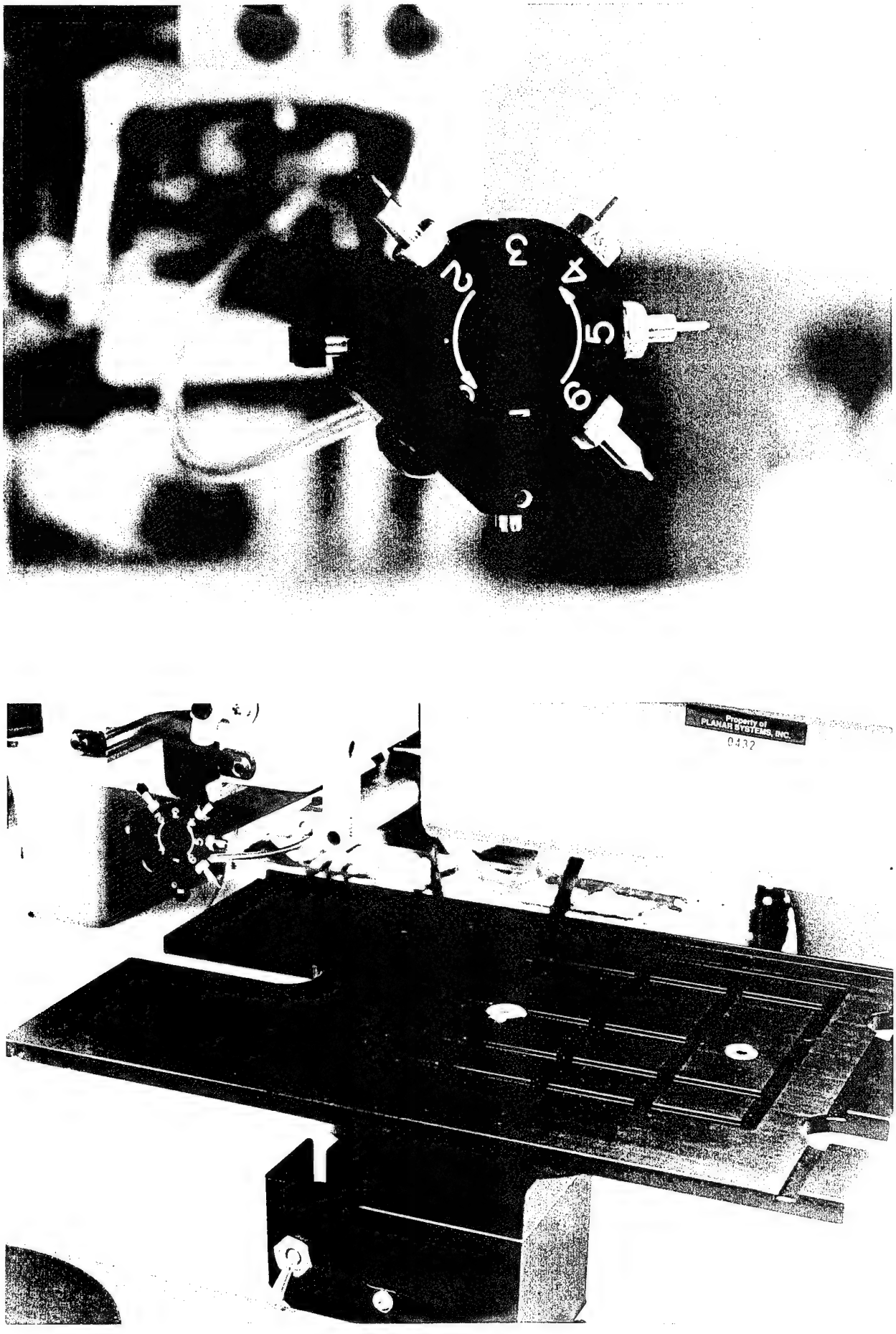
## Appendix A: Photographs



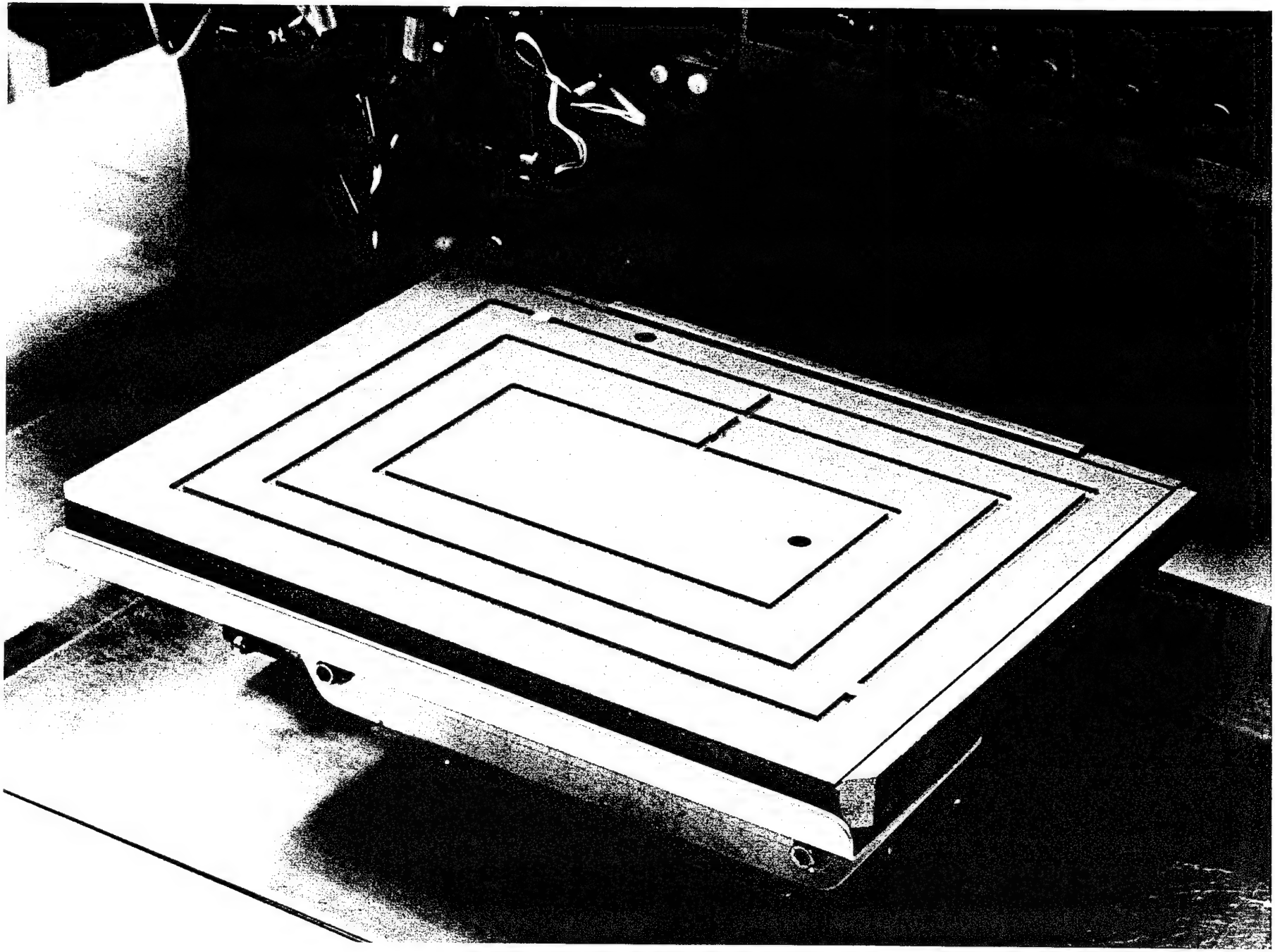
**PHOTOGRAPH A1.** Hughes 2500-II die bonder and Hughes 2460-III gold ball bonder under Laminar Flow Hood.



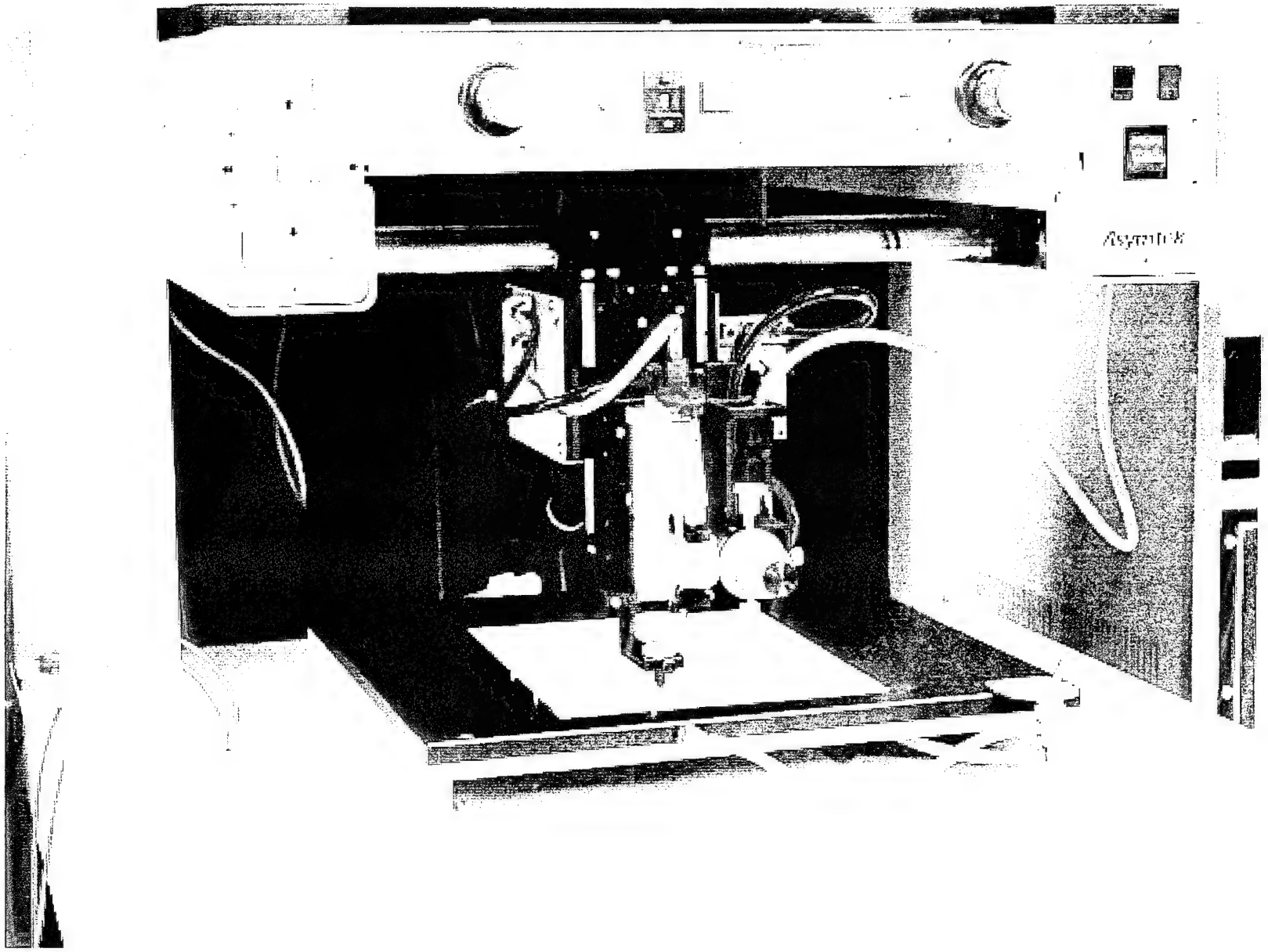
**PHOTOGRAPH A2.** Asymtek A402G encapsulation machine flanked by two Blue-M curing ovens.



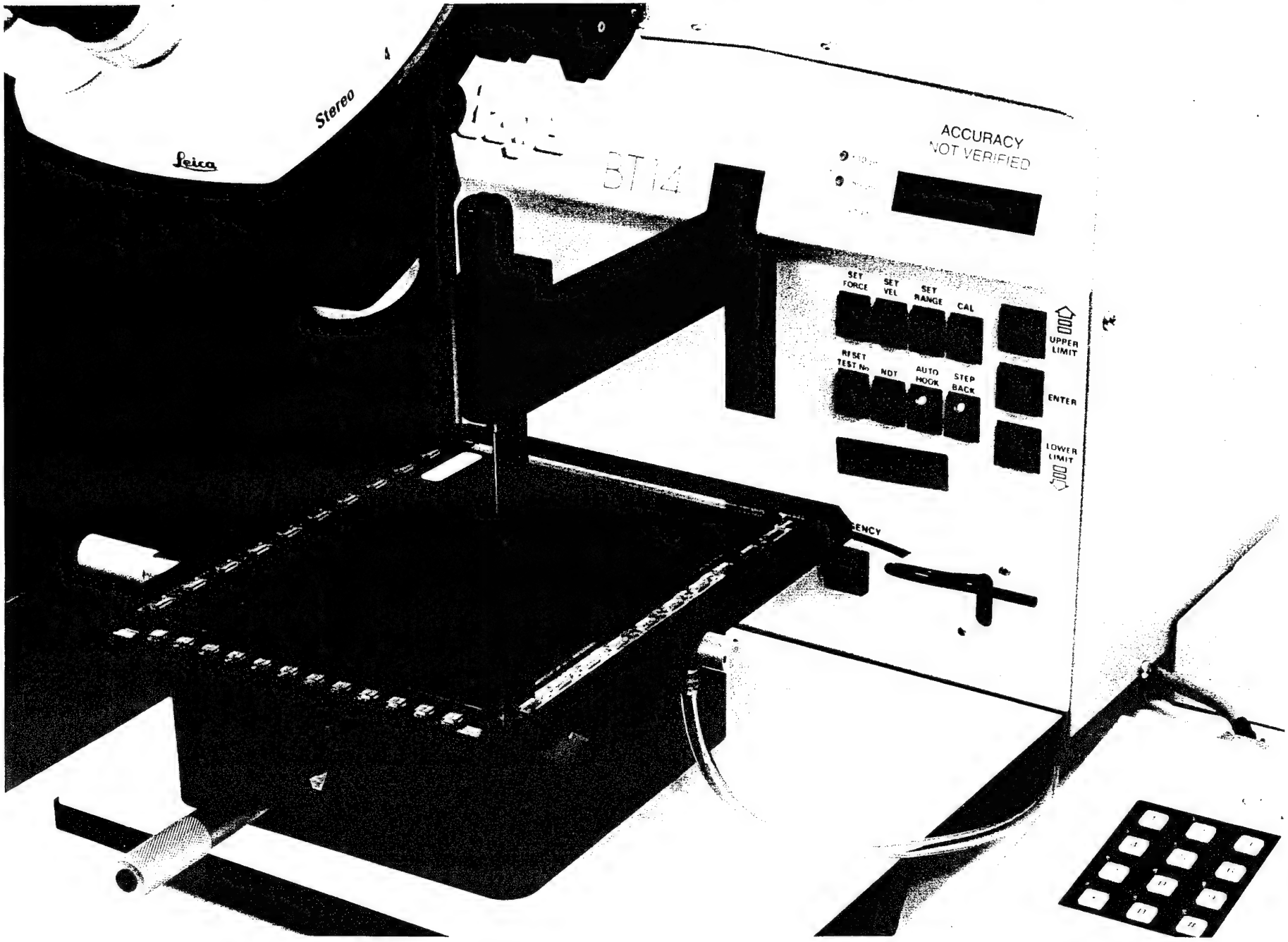

**PHOTOGRAPH A3.** Top photo is custom die pickup tool and the bottom photo is the rotating glass fixture, both for the Hughes 2500-II.



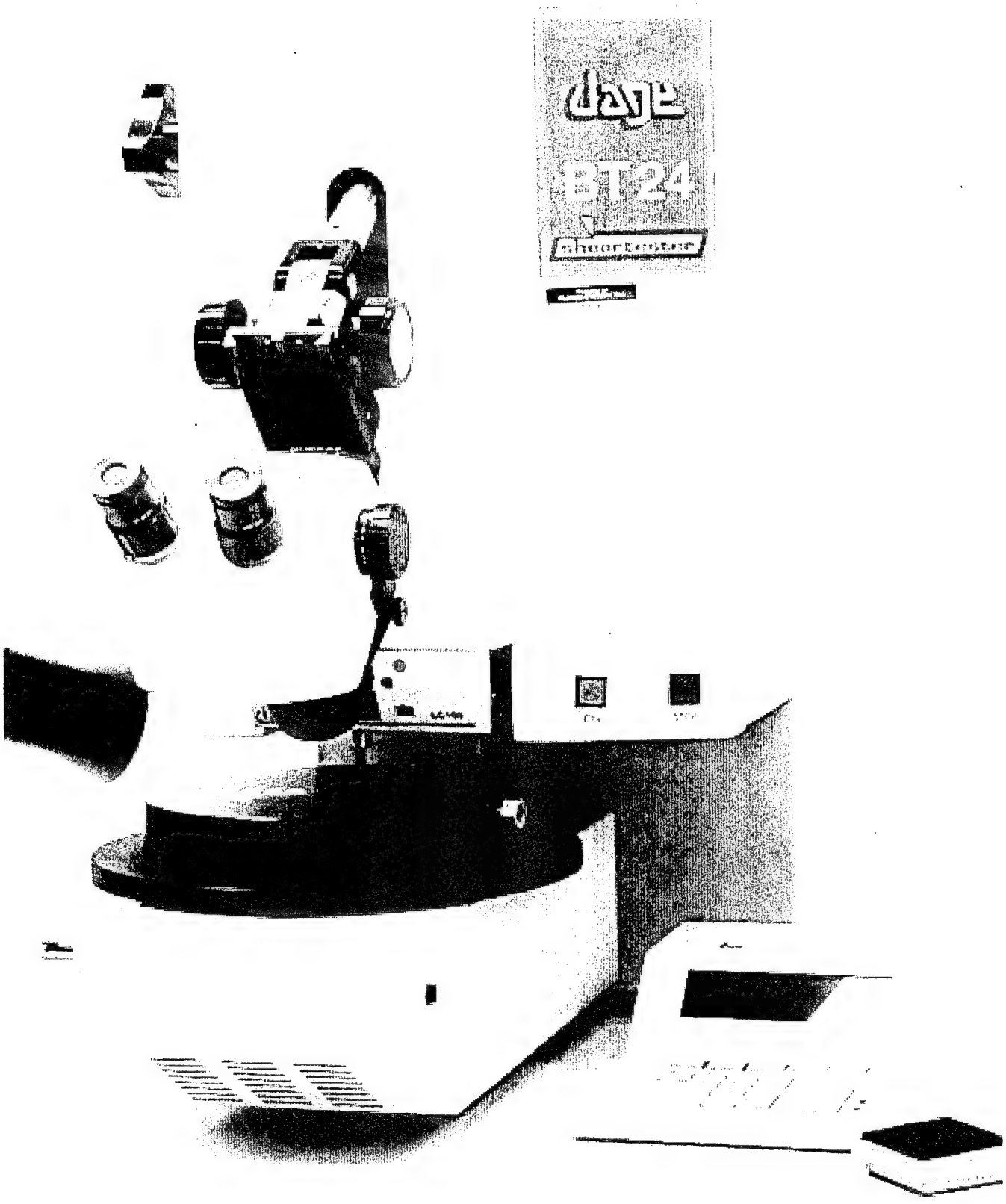
**PHOTOGRAPH A4.** Oversize heater stage on the Hughes 2460-III.



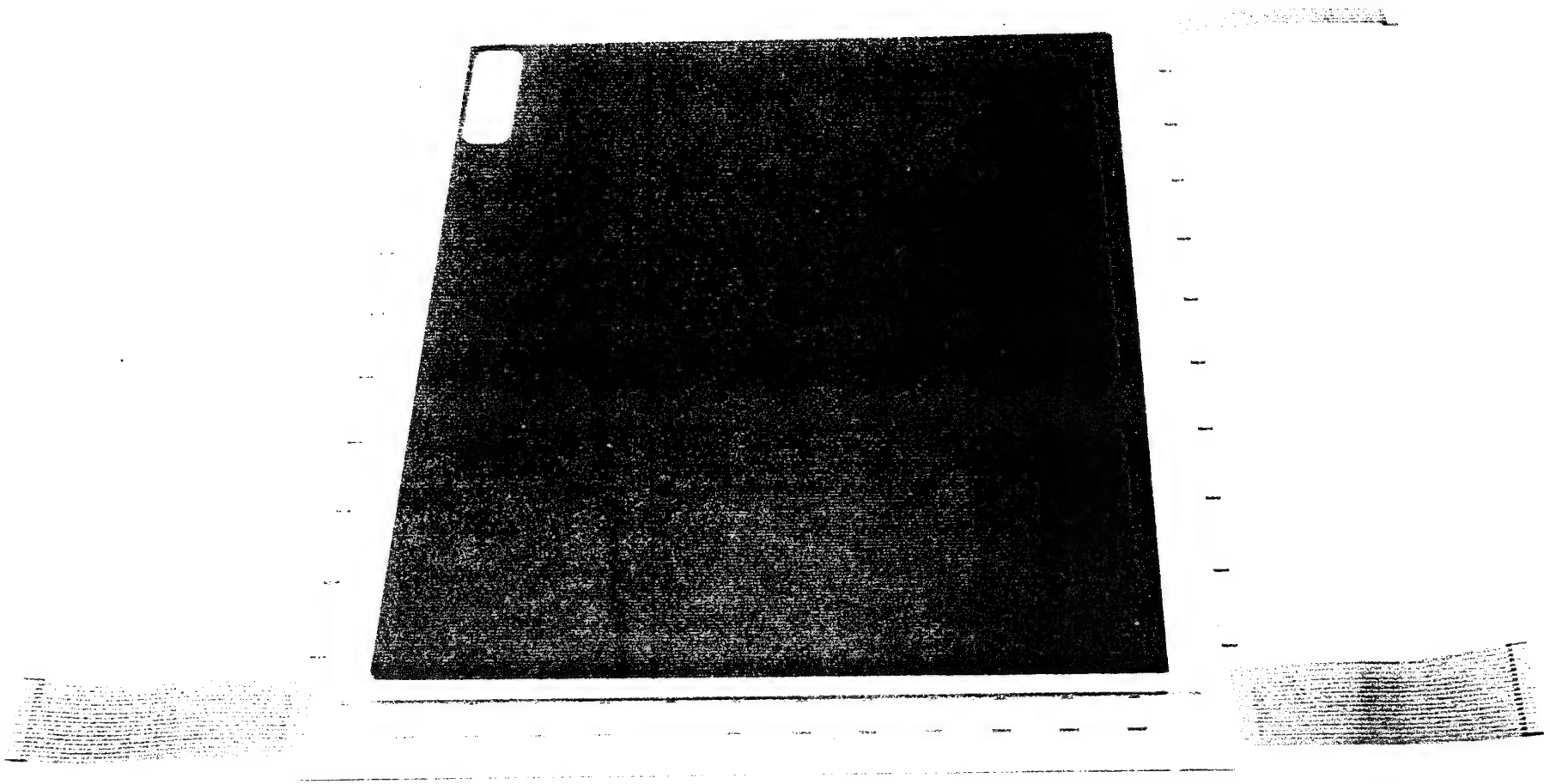
**PHOTOGRAPH A5.** Asymtek A402G encapsulation machine with dual toggle head assembly



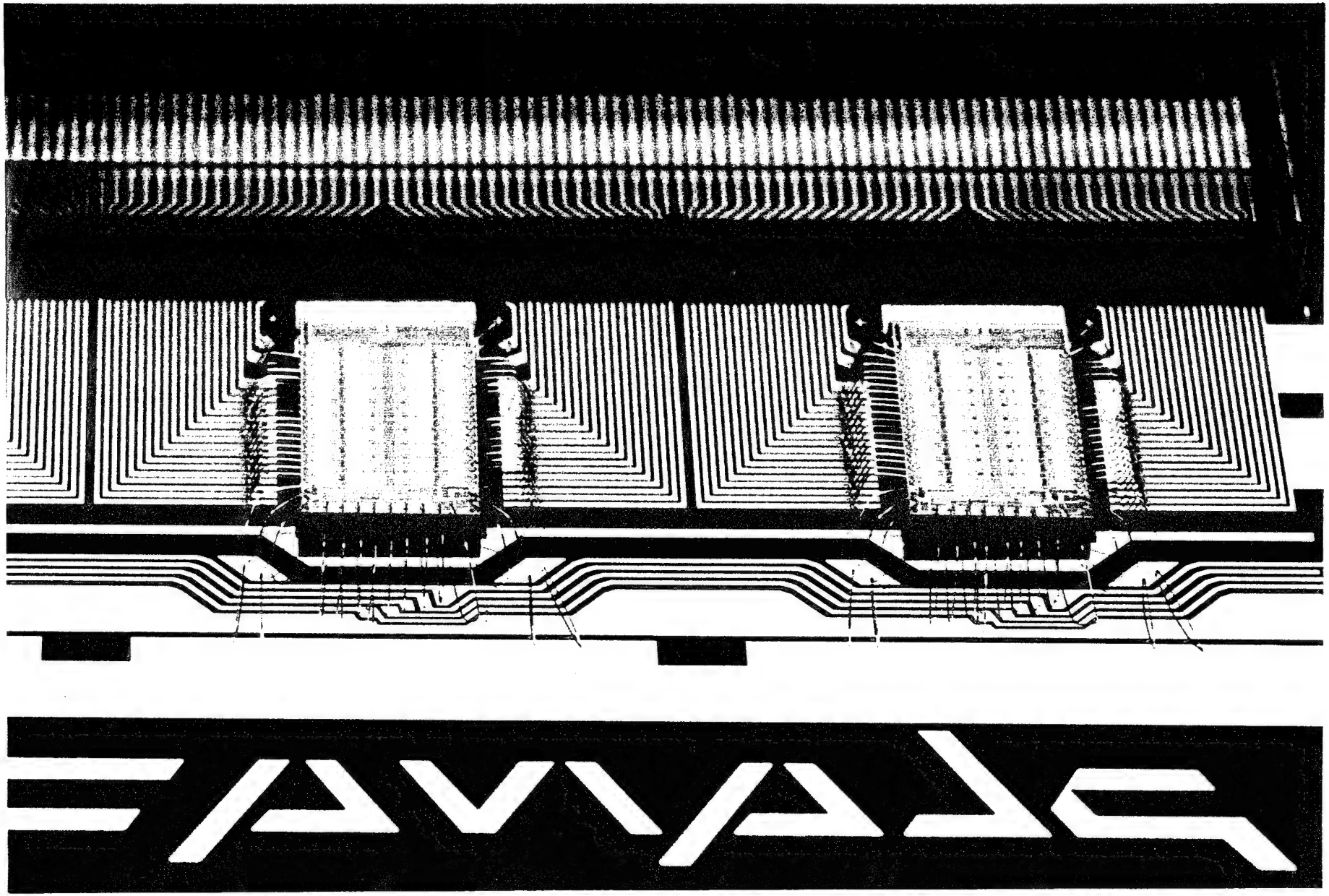

**PHOTOGRAPH A6.** Dage BT-14 wire bond pull tester.



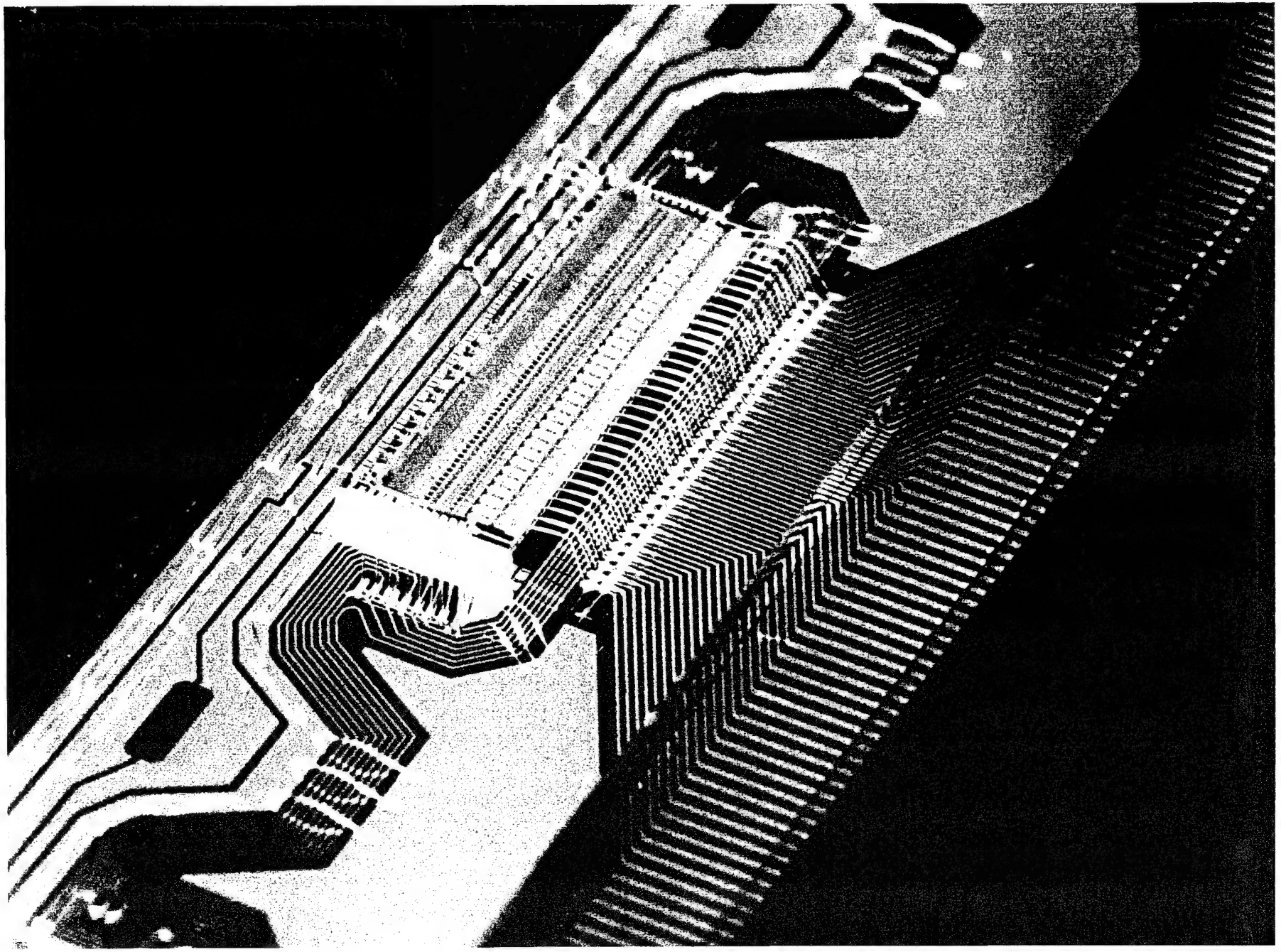

**PHOTOGRAPH A7.** Dage BT-24 ball bond shear tester.



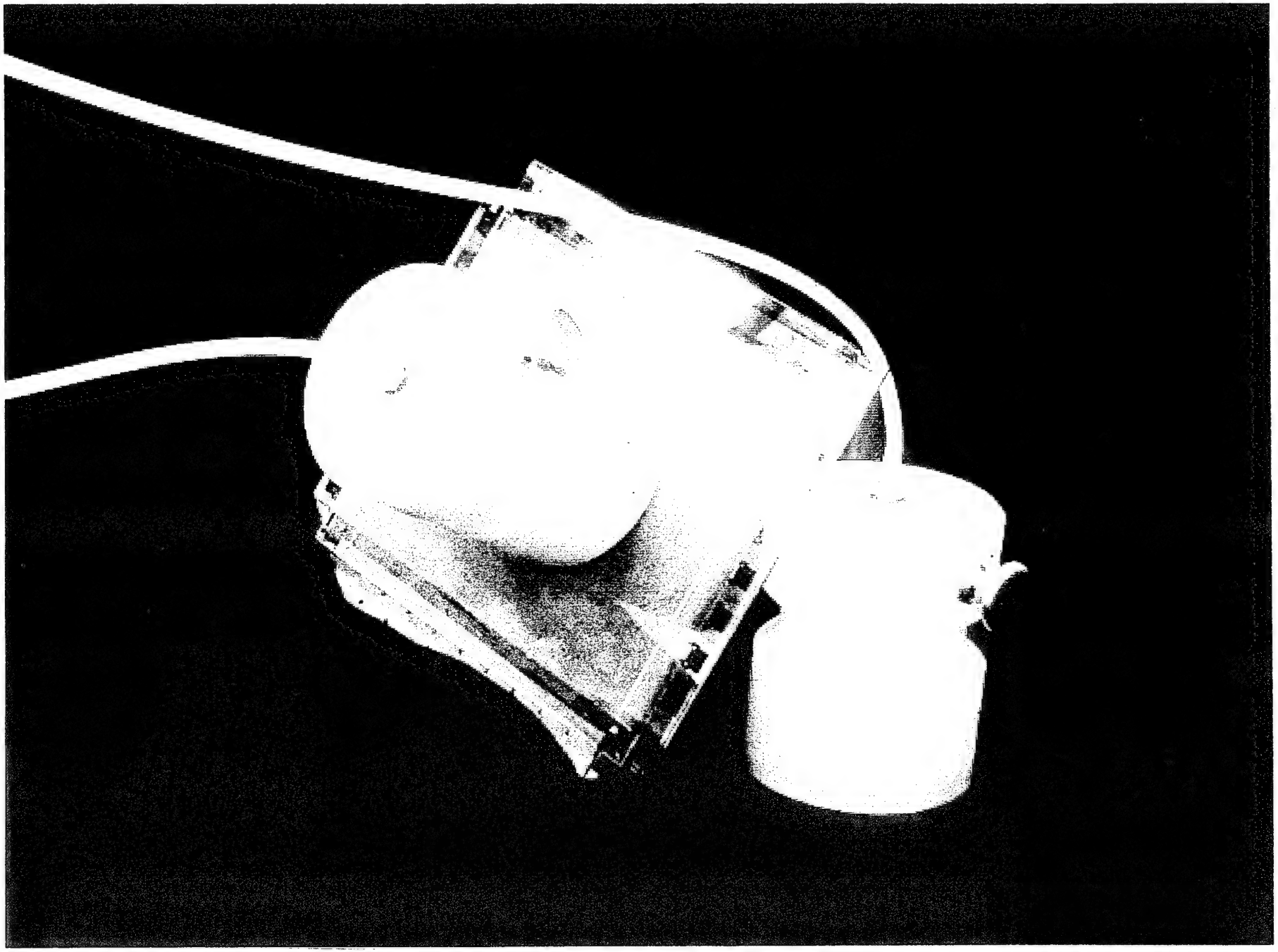
**PHOTOGRAPH A8.** Monochrome VGA display using COG drivers.



**PHOTOGRAPH A9.** HV72 row driver IC and bus on the monochrome VGA display.

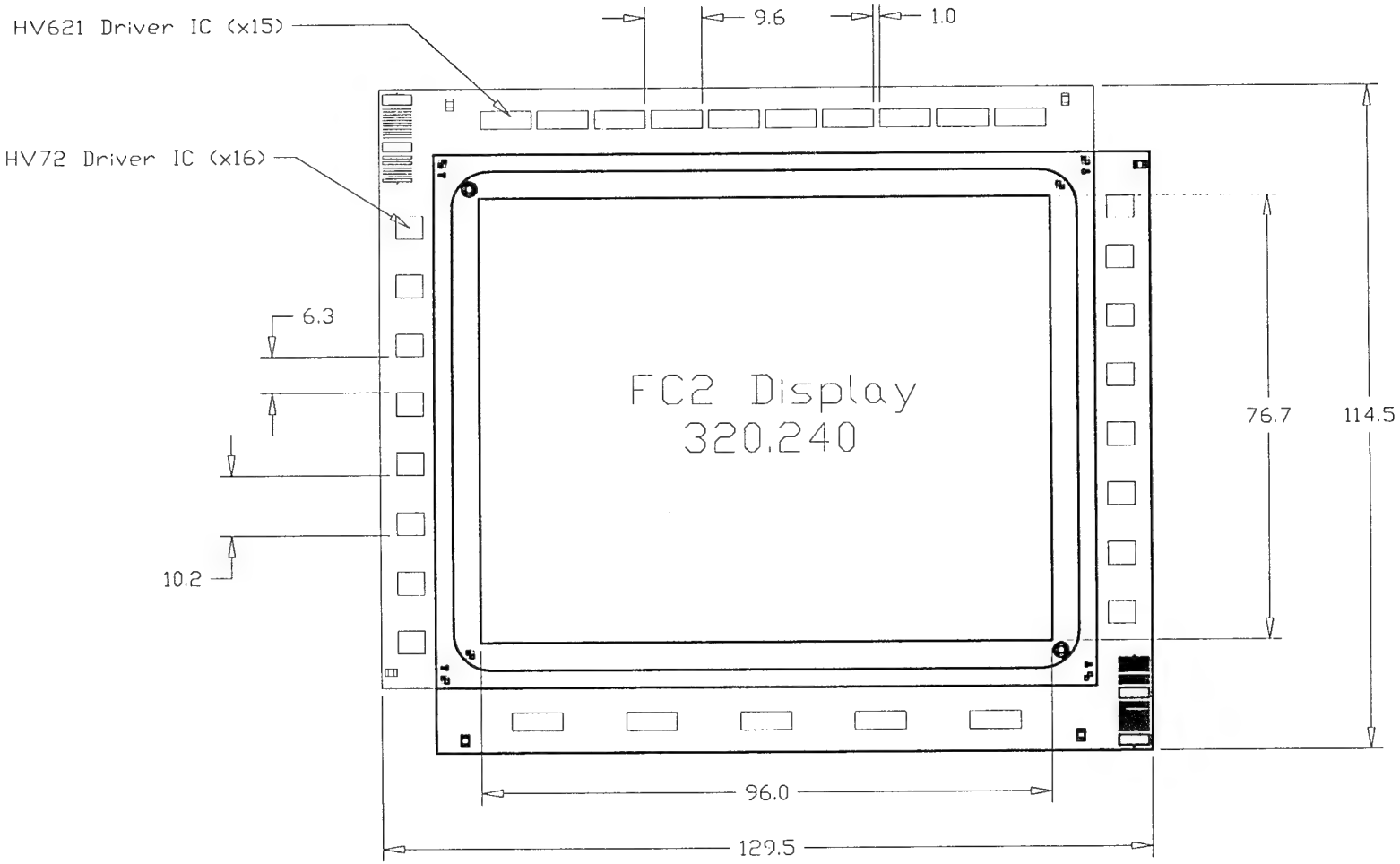


**PHOTOGRAPH A10.** HV621 column driver IC and bus on the monochrome VGA display.

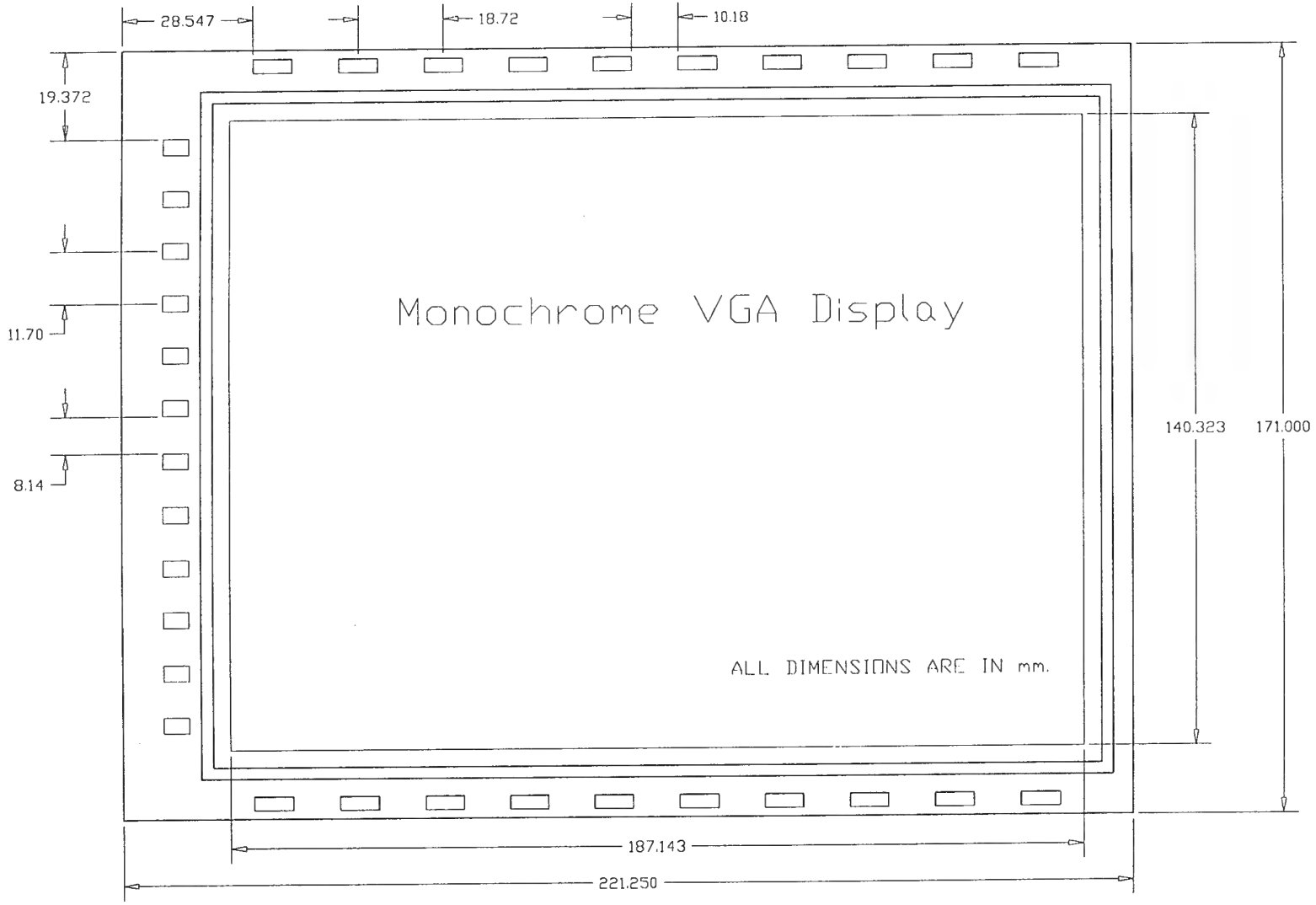


**PHOTOGRAPH A11.** Pucks for rotating and flipping hot glass.

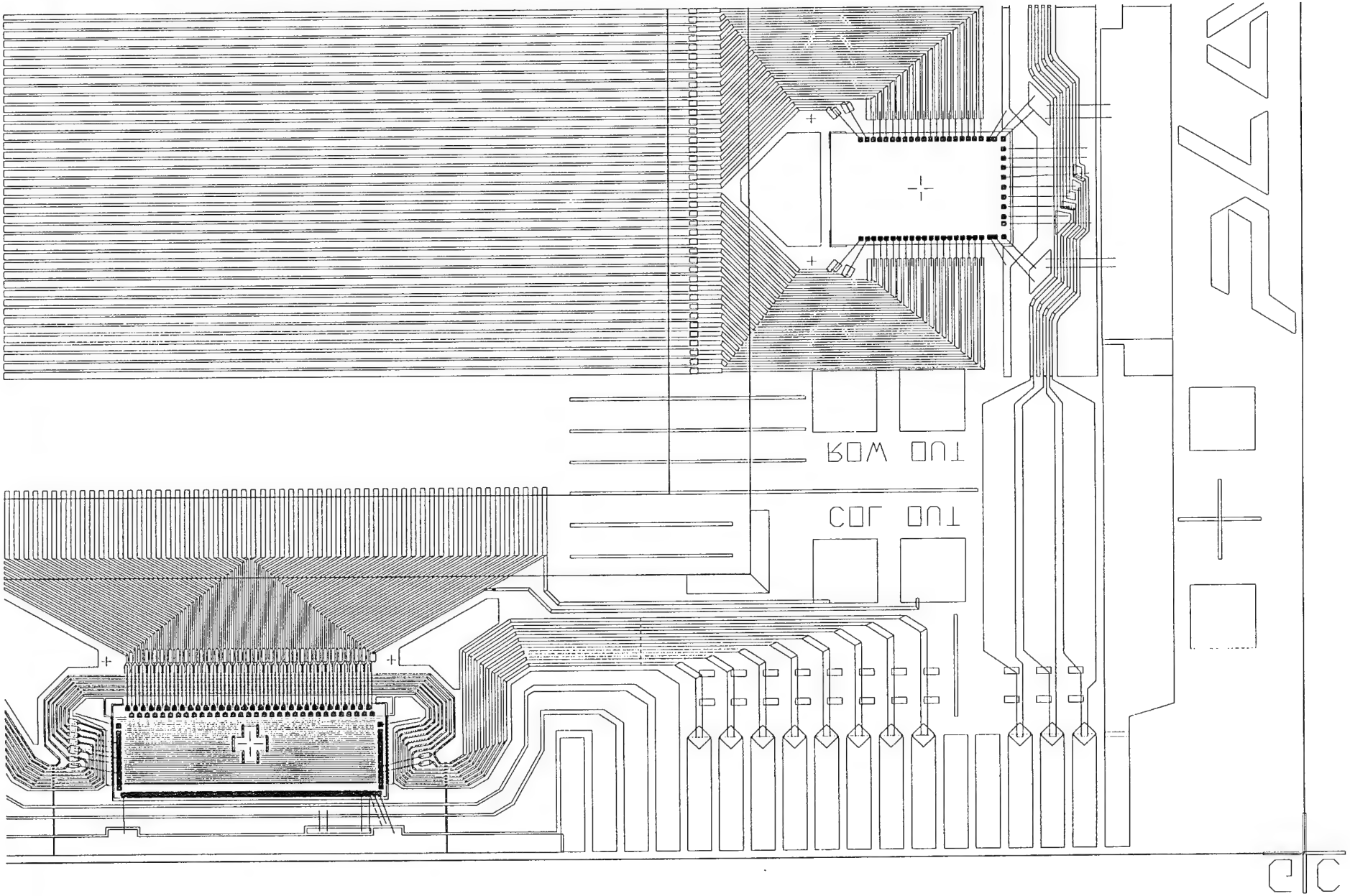
## Appendix B: Drawings



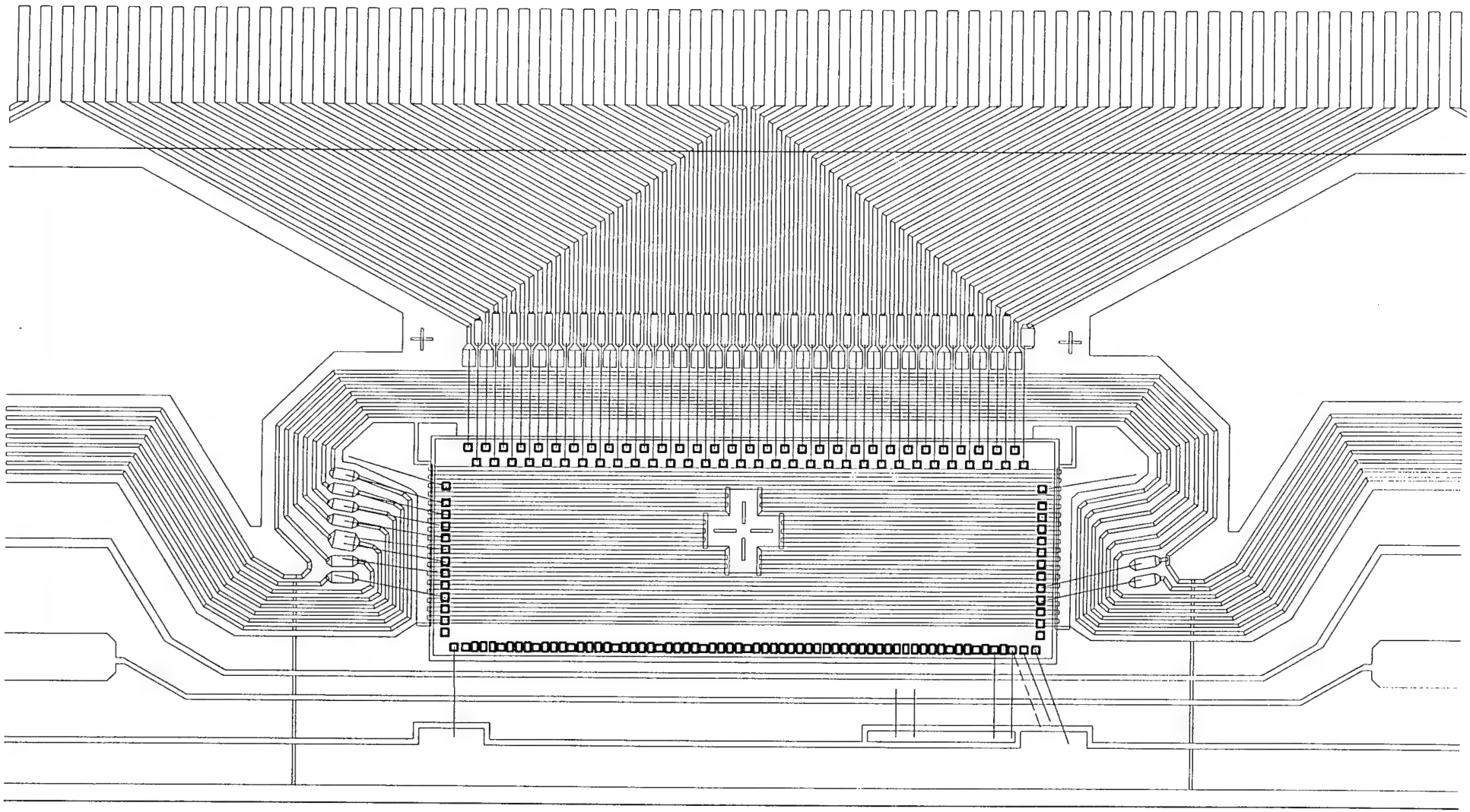

**DRAWING B1.** The 1/4 VGA (FC2) Display Mechanical Dimensions.



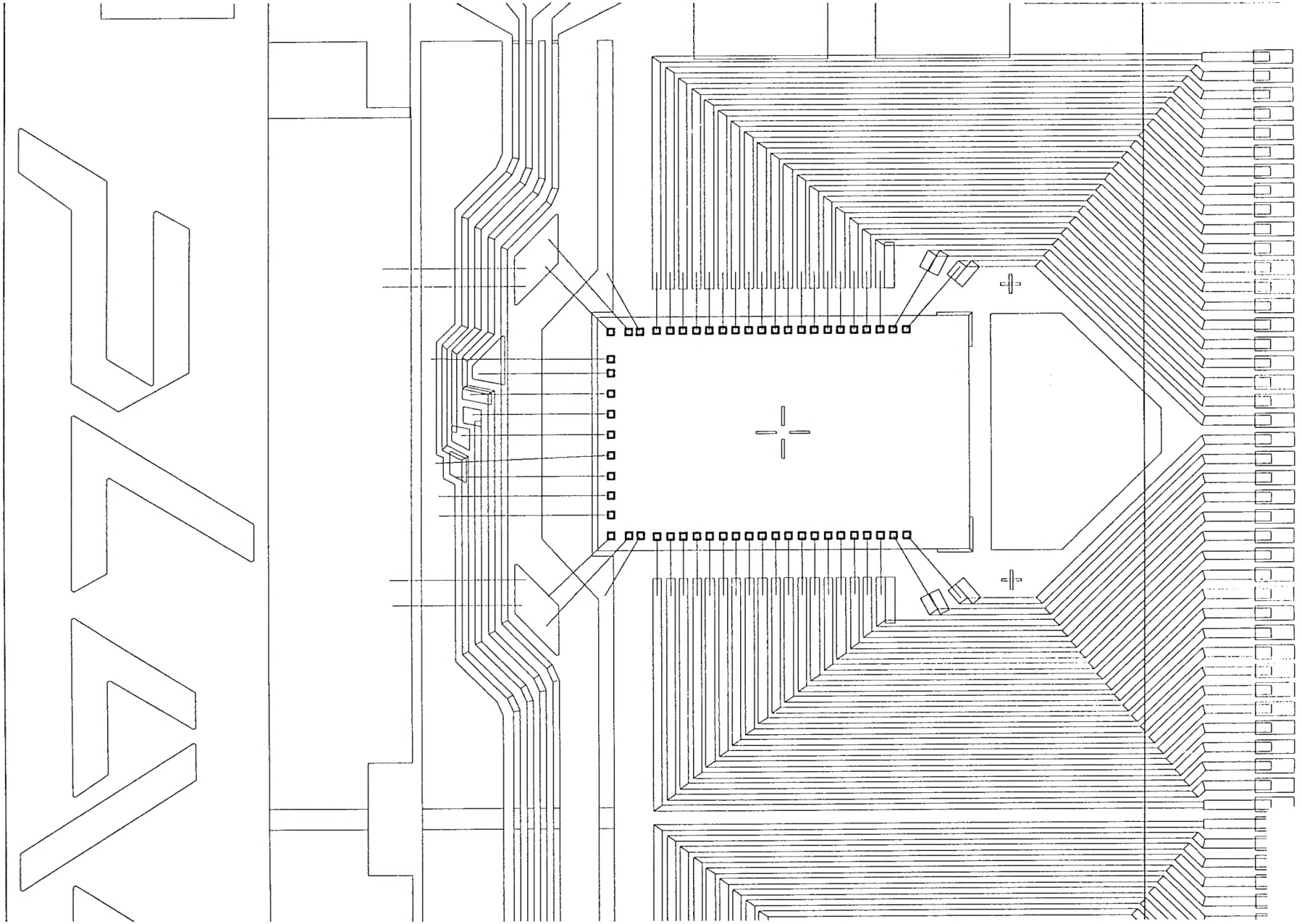

**DRAWING B2.** Monochrome VGA Display Mechanical Dimensions.



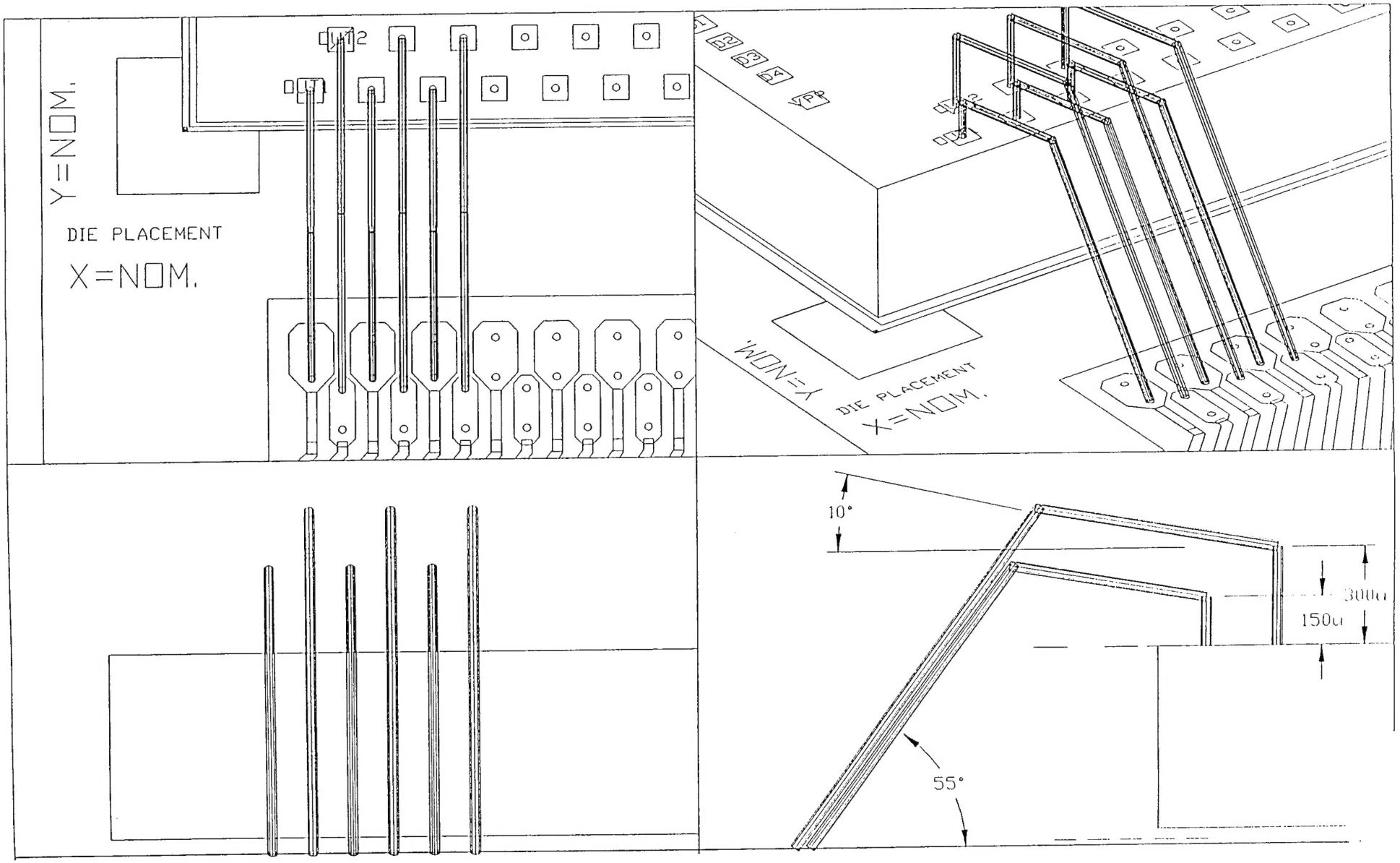

**DRAWING B3.** Column driver, row driver and cable foot print on the Monochrome VGA Display.



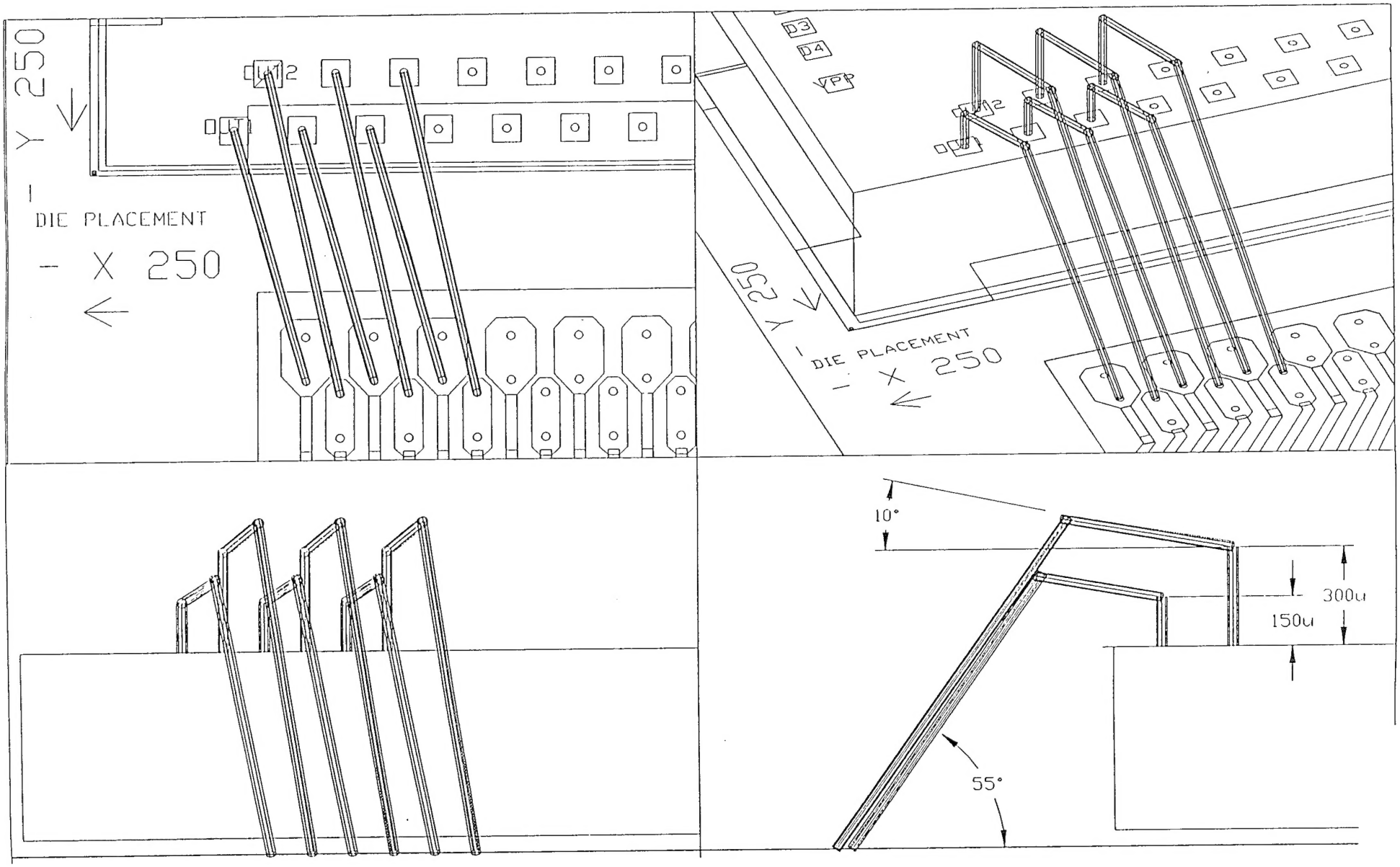
**DRAWING B4.** Column driver (HV621) with wires and bus structure.



**DRAWING B5.** Row driver (HV72) with wires and bus structure.




**DRAWING B6.** View of column driver wire bonds at 120um pitch, at nominal die placement.




**DRAWING B7.** View of column driver wire bonds at worse case die placement (+/- 250um).

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